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Section 7: Non-crystalline materials

ELECTRICAL PROPERTIES OF LPCVD POLYSILICON DEPOSITED IN THE VICINITY OF AMORPHOUS – POLYCRYSTALLINE PHASE

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Using dark d.c. electrical measurements, the electrical properties of LPCVD polysilicon deposited at 570 °C and 620 °C are studied. The grain boundaries are assumed to be described with disordered material and applying the Mott's theory, the density of states near the Fermi level was determined, obtaining the values $3.78\cdot10^{18}$ cm^{-3} and $1.40\cdot10^{18}$ cm^{-3} for the samples deposited at low temperature and for those deposited at 620 °C, respectively. Various behaviours are found if the samples are annealed. After annealing the samples deposited at 570 °C prove an increasing of the amorphous component represented by the grain boundaries, while for samples deposited at 620 °C the same annealing process produces an increase of the crystalline part. The super-coordination defects produced and the passivation effects given by the annealing in hydrogen atmosphere are used to explain these transformations. The conduction mechanism is controlled by the grain boundaries's properties.

Keywords: Polysilicon, LPCVD, Annealing, Conductivity, Grain-boundaries

1. Introduction

Polycrystalline –silicon (polysilicon) films obtained by chemical vapour deposition are used in a wide variety of VLSI applications requiring very different electrical properties. The undoped and light doped layers show a high resistivity and are used in the fabrication of the high – value load resistors for static RAM cells memory. The highly doped polysilicon films are characterised by a low resistivity, but limited by the amount of the dopant that can be incorporated in substitutional site in the grains. Due to its electrical and optical properties, the polycrystalline silicon is used in many applications as: i) in integrated circuit technology as passive elements, ii) in large-area liquid crystal displays as thin film transistors (TFT) used as switching elements, iii) in the solar cells technology as performant material to produce solar cells with high conversion efficiency and low- cost, etc.

The polysilicon structure, represented by size and number of the crystalline grains, has a great influence on the physical properties of the material. Thus, the resistivity is related to the grain boundaries and by controlling the number of grain boundaries or their electrical activity it can modify the electrical properties of such kind of layers. There are studies on LPCVD polysilicon films prepared from silane where the correlation between crystalline structure and deposition parameters is established. Thus, the temperature, deposition pressure, deposition rate and the dopant determine the polysilicon grain structure [1-3].

In this paper we study the electrical properties of undoped LPCVD polycrystalline silicon deposited at 570 °C and 620 °C. It is shown by Hasataka [4] that the deposition temperature 580°C is a demarcation limit between the amorphous phase and polycrystalline phase. This temperature value should be understood as one depending also to other deposition parameters. In order to understand the structural differences of these two depositions, we have studied both the as deposited and annealed samples's states. The annealing of the samples has a major effect on the grains size and electrical properties.

2. Sample preparation and characterisation

The polycrystalline thin films were deposited by thermal decomposition of pure silane in a standard, horizontal hot-wall ASM LPCVD reactor provided with automatic control of flow rates, temperatures and pressures. The quartz tube length was 2000 mm while de diameter was 130 mm. The silicon wafer substrates covered by a 1000 – 1030 nm silicon dioxide layer were located in the hot region of the tube (the middle zone). Polysilicon depositions were done at the same pressure value (0.4 Torr) for two temperatures: 570 °C (samples 570FS and 570AS) and 620 °C (samples 620FS and 620AS). Part of samples was measured like as deposited samples (labelled with FS) and part of them was annealed at 350°C for 30h in H_2+N_2 (1:3) atmosphere (labelled with AS).

The d.c. electrical measurements were performed on the coplanar structures obtained by thermal evaporation of aluminium on the top of polysilicon layers, using a shadow mask with 0.5 mm gap between electrodes. The aluminium pad dimensions were 3x4 mm^2. Current – voltage characteristics were performed in a classical d.c. system in vacuum under dark conditions. The applied voltage was varied between 0.5 V and 20 V at room temperature. Keeping dc bias constant, V = 5 V, the temperature was varied in steps of 10 K from 223 K to 415 K. The temperature was measured with a cromell – alumel thermocouple placed close to the sample on the copper sample holder.

3. Basic considerations on the conduction mechanisms in polycrystalline semiconductors

Generally, the polycrystalline materials are composed from small crystallite surrounded by grain boundaries. The grain boundaries are assumed to be narrow compared to the size of the grains. They will act as carrier traps, affecting the transport of charge carriers. In the most part of the models that describe the transport mechanisms into polycrystalline silicon, the grain boundaries are considered to have wideness of a few lattice constants and a higher band gap in comparison with the crystalline silicon. The grains' sizes are various and the barriers between grains can be different. It was shown that the grain size varies through the film thickness, being greater near the top than near the bottom.[1] As normal, the current flow will be along the lower resistance, the transport of the carriers being a percolation of the most conductive path. In other words, in such kind of materials, the current is a non-linear function of the applied voltage.

Elaboration of a transport model taking into accounts a statistical description of the grain size distribution is complicate and many times inefficient, because this distribution depends sensitively on the conditions of deposition which vary so much from one reactor to another. From this point of view, the solution adopted was to consider uniform grain size. For simplicity, it is assumed [5-7] that the polycrystalline materials are composed of N_g grains of average size L and the grain boundaries are perpendicular to the current direction. Due to the highly disordered nature of the grain boundaries and the number of the trapping states, which characterise these regions, they play an important role in the electrical conduction mechanism. The nature of the grain boundary was considered to be either between that of a completely ordered single crystal and that of a highly disordered amorphous material [6] or a very amorphous material [8]. Due to fact that the disordered material has an optical gap much larger than the energy gap of the single-crystal from crystallites, a heterojunction is formed at the grain/grain-boundary interface. Under these conditions, potential barriers are used in order to model these intern interfaces. The carriers must either tunnel through the grain-boundary barrier or to jump over it, in order to move from one crystallite to another.

A very interesting result obtained by Mandurah et al. [6] on the transport particularities of the polycrystalline silicon is related with the average resistivity ρ given as:

$$\rho = \frac{L_c}{L}\rho_c + \frac{L_{gb}}{L}\rho_{gb} \tag{1}$$

where ρ_c and ρ_{gb} are the resistivities of the grain (crystalline part) and grain boundary respectively. In the Eq. (1), L is the average total length of a grain – grain boundary cell ($L = L_c + L_{gb}$), L_c is the width of the undepleted region of the grain, while L_{gb} is formed by the grain boundary width and the

adjacent depleted regions in the grain. Working in an unidimensional model, we can consider that the conductivity, σ, is related to the resistivity by $\sigma = \rho^{-1}$. One assumption that we do is to consider that all L_{gb} has the conductivity σ_{gb}. Under this condition, we define as crystalline fraction, $f_c = L_c/L$ and amorphous fraction, $f_{gb} = L_{gb}/L$, of course, taking into account that $f_{gb} + f_a = 1$. Using this notation, after some simple mathematics, the Eq. (1) becomes:

$$\sigma = \frac{\sigma_c}{1 + f_{gb}\left(\frac{\sigma_c}{\sigma_{gb}} - 1\right)} \tag{2}$$

This result is in good agreement with that one given by Kim et al. [8] using their model for a small signal theory for dc conduction defining a crystalline – amorphous – crystalline (C-A-C) cell structure. Considering that the current in the C –A – C structure is due to the drift and diffusion of the carriers, hence due to the local slope of the quasi-Fermi level, they have obtained the current density through this cell, for undoped polysilicon, as:

$$J = qp_i \frac{\mu_c}{1 + \frac{\delta}{L}\left(\frac{\mu_c p_i}{\mu_{gb} p_{gbi}} - 1\right)} \cdot \frac{V_a}{L} \tag{3}$$

where: V_a is the voltage across each crystalline-amorphous cell of length L, δ is the grain boundary width, μ is the carrier mobility, p_i is the holes density (c and gb label crystallite and grain boundary, respectively) and q is the electron charge. In fact, Eq. (3) express the current density by an effective mobility. Taking into account that the ratio V_a/L is the electrical field strength, F, we can see that:

a) if we define the conductivity of the crystalline / amorphous parts as $\sigma_i = qp_i\mu_i$ and $f_{gb} = \delta/L$, the Eq. (3) could be rewriten as $J = \sigma \cdot F$, where the σ is expressed by Eq. (2);
b) for undoped polysilicon there is the linearity $J \propto F$.

As concerning the temperature dependence of the conductivity of the grain boundary part, in the light of the Mott's model for amorphous semiconductors [9] we have to distinguish two principal dependences:

i) for high temperature range

$$\sigma = \sigma_o \exp\left(-\frac{E_\sigma}{k_B T}\right) \tag{4a}$$

if the measurement temperature, T, is enough to activate the transport mechanisms from and to the extended states that define the valence and conduction – band, respectively. In Eq. (4a), E_σ is the thermal activation energy of the process and k_B is the Boltzmann's constant;

ii) for low temperature range, the percolation theory of the hopping conduction on the localised states near the Fermi level gives:

$$\sigma_{gb} = \frac{A}{\sqrt{T}} \exp\left[-\left(\frac{T_0}{T}\right)^{1/4}\right] \tag{4b}$$

where A is a constant of the model and $T_0 = 18\alpha^3 / \left[k_B N(\varepsilon_F)\right]$ allows us to the determine the density of the states localised at the Fermi level, $N(\varepsilon_F)$, if α (the coefficient of exponential decay of the localised states wave function), is known.

4. Experimental results

Current-voltage characteristics of studied polysilicon samples were carried out. In Fig.1 is shown the current density – electric field characteristics (j – F), in logarithmic scale. The dot line represents the $j \propto F$ plot, which is done here, as an eyes guide, proving that for the most part of the applied electrical field, the Ohm's low is available. With these experimental data, the electrical

conductivity, σ, is $2.63\times10^{-5}\ \Omega^{-1}cm^{-1}$ for sample deposited at 570°C and $3.47\times10^{-4}\ \Omega^{-1}cm^{-1}$ for sample deposited at 620 °C. After annealing, σ becomes $3.65\times10^{-6}\ \Omega^{-1}cm^{-1}$ for sample 570AS and $8.41\times10^{-4}\ \Omega^{-1}cm^{-1}$ for sample 620AS, respectively. As it can be observed, the annealing process, given on the same conditions, decreases the conductivity of samples deposited at 570 °C and increases that of samples deposited at 620 °C.

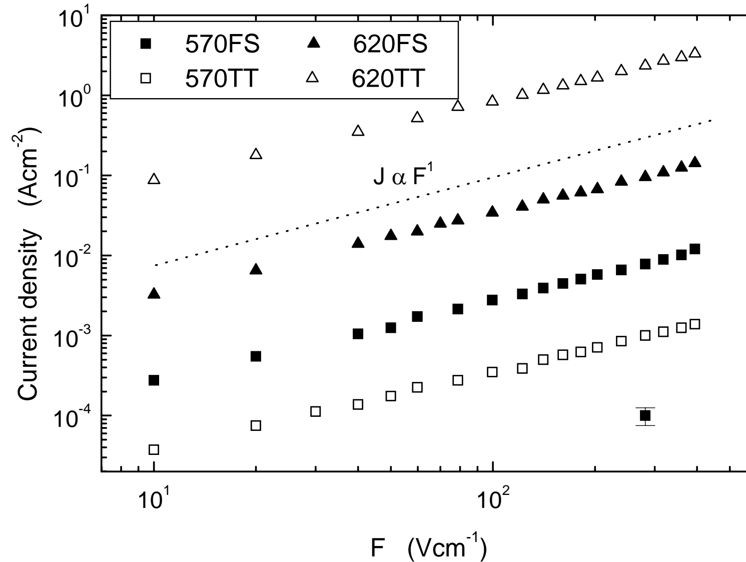

Fig. 1. Current density versus the electrical field strength. The dot line done as an eye guide,

describes J∝F.

Keeping constant the electric field at the value 100 Vcm^{-1}, the dependence of the conductivity on temperature, is given in Fig. 2. The plot is done in standard semilogarithmic scale, with σ versus $10^3/T$. Two regions for all samples are clearly distinguished: one in the high temperature range, which represents a thermal activated conduction process and the second one in the low temperature range, where in our opinion, the dangling bonds which characterise de grain- boundaries determine a hopping transport process. In fact this process could also be at high temperature, but there the high conduction channels offered by the thermally excited path, over the barrier mask it. The values of the thermal activation energy, E , determined from the high temperature region are given in table 1. One can see, that the annealing process affects the E parameter, for the two deposition temperatures, after annealing the thermal activation energy is higher as compared with it's initial value.

Table 1. Thermal activation energy and dangling bonds density of states in the grains Boundaries.

	570FS	570AS	620FS	620AS
E (eV)	0.45	0.62	0.48	0.55
$N(\varepsilon_F)$ (cm^{-3})	3.78×10^{18}	6.60×10^{18}	1.40×10^{18}	5.33×10^{17}

Mott's plots specific to the low temperature measurements in the amorphous materials, $Ln(\sigma T^{1/2}) = f(T^{-1/4})$, are presented in Fig.3. A good linearity is observed for all samples and assuming the coefficient α to be 1.24 nm^{-1}, [10], the density of states localised near Fermi level, $N(\varepsilon_F)$ can be calculated. The values are listed in table 1. Samples as-deposited show a lower dangling bonds density when the deposition temperature is higher. With annealing, sample low temperature deposited points out an increased defect density whereas those deposited at 620°C decrease this parameter.

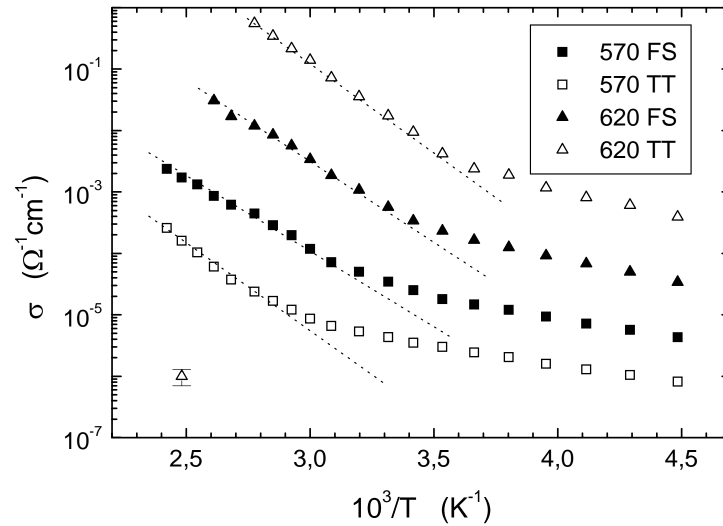

Fig. 2. Electrical conduction variation with the inverse temperature for both as-deposited and annealed samples.

5. Discussions

As the Fig.1 shows, all our undoped polysilicon samples are characterised by a linear shape of the current density versus electrical field strength for both of them, as deposited or annealed samples. This is in good agreement with Kim's theoretical model of the electrical conduction in undoped polysilicon (Eq. (3)). We have shown in Section 3 the important role played by the grain boundary structure on the charge carrier transport. It is known that traps are associated with the dangling bonds at the grain boundaries arising from the lattice discontinuities. The improvement of the conductivity values is related to the passivation of these dangling bonds. Hydrogen atoms can passivate dangling bonds or other defects formed when differently oriented grains join. One other idea to reduce the active trap density is to remove the grain boundaries by annealing techniques. Of course, as the number of traps is reduced, the number of trapped carriers decreases. Using the annealing process at 350 °C in hydrogen atmosphere, we have tried to obtain, on the same time, high dimension for the crystalline grains and a good passivation of the dangling bond sites. Annealing at low temperature can also move the hydrogen to the grain boundaries where it reduces the traps' effectiveness.

Looking on the results from Fig. 1, we can see that this purpose was reached only for samples deposited at 620°C. For those, the conductivity was increased with a factor of two. As the Eq. (2) shows, the smaller amorphous fraction, the higher is the conductivity of the material. In the other words, the annealing process has increased the fraction of the crystalline part. Then, taking into account that high grain size means a smaller contribution of the grain boundaries, we can conclude for the samples deposited at 620 °C and annealed, that the dangling bonds' number decreases. Using the Eq. (4b), which describes the temperature dependence of the disordered regions' conductivity, in the Fig. 3 are plotted the σ's experimental values on the so-called Mott's plot. The density of states localised near the Fermi level, which allow a tunnelling conduction path, by energy percolation, can be determined from the plot slope. As is given in the table 1, $N(\varepsilon_F) = 1.4 \cdot 10^{18}$ cm^{-3} that was found for as-deposited sample, is decreased to $N(\varepsilon_F) = 1.4 \cdot 10^{18}$ cm^{-3}.

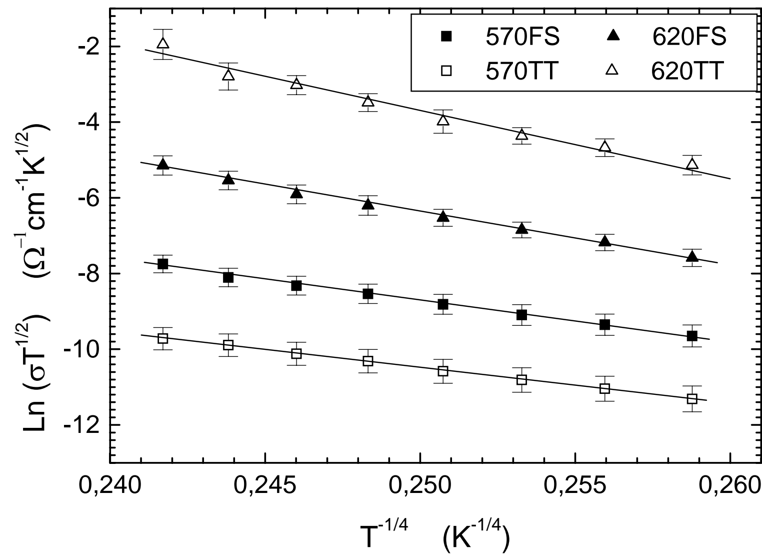

Fig. 3. Mott's plots for low temperature values region. Symbols are experimental data and the straight lines represent the fits with the Mott's law from amorphous semiconductors.

More than this, at high temperature measurements, the thermal activated conduction mechanism is shown in the Fig. 2 where, the slope of the $\lg(\sigma) = f\left(10^3/T\right)$ yields an $E_\sigma = 0.48$ eV for sample as deposited and $E_\sigma = 0.55$ eV for annealed sample. Both of these values are the results of a mathematical expression as the Eq. (4a) corroborated with Eq. (2). Even thought, the σ_c 's temperature variation is well defined in the crystalline silicon theory and experiment, the variation of the global conductivity with the measurement temperature is not yet completely understand. The fraction of the disordered material is modified by the annealing process, but is also changed the traps' efficiency of dangling bonds. Under these conditions we suppose that for samples deposited at 620°C the decrease of the dangling bonds' number and the increase of the thermal activation energy values are given by a more crystalline quality of the annealed material.

Looking for the same physical amount determined for samples deposited at 570°C, we could see that by annealing the dangling bonds' number is increased (practically doubled). This means that the grain boundaries' weight on the whole material structure is higher for the annealed samples. A good support for this idea is given by the conductivity values at room temperature that changes from $2.63 \cdot 10^{-5}\ \Omega^{-1}cm^{-1}$ before annealing to $3.65 \cdot 10^{-6}\ \Omega^{-1}cm^{-1}$. We suppose that during annealing process, the grains are broken. One interstitial hydrogen atom could interact with bonded silicon atoms and spread this bond. The interaction is higher when the temperature is higher and, due to the local temperature fluctuations, the bond is broken. This mechanism is known in the amorphous material physics as one way to produce super-coordination defects. Energetically, these defects give states near Fermi level. Under such circumstances, the amorphous part contribution to the electrical conductivity increases and a higher number of dangling bonds' defects obtained for sample 570AS, in comparison with sample 570FS, is explained. On the other hand, breaking the crystalline grains, the amount of the material disorder is increased, which means a wider tail of localised states for valence and conduction bands.

Why this various behaviour for samples deposited at 570 °C in comparison with that deposited at 620 °C? It could be related to the different structure of the produced layers. As the conductivity values and the dangling bond number confirm, the samples deposited at lower temperature have more amorphous part. It was shown, [3], that crystalline entities appear also in low deposition temperature LPCVD; and this is supported by our electrical data. It seems that the cohesion

of these entities is lower for samples deposited under amorphous –polycrystalline phase temperature which is 580 °C [4].

6. Conclusions

The electrical properties of the polycrystalline silicon produced at 570 °C and 620 °C have been investigated and have been shown to be functions of the electrical properties of the grain boundaries. The principal ideas of this paper can be summarised as following:

i) for undoped polysilicon LPCVD sample the current density depends linearly on electrical field intensity across the sample;

ii) samples deposited at 620 °C show a higher crystalline material fraction having a higher electrical conductivity;

iii) the annealing process done in hydrogen atmosphere have increased the density of states near the Fermi level and the resistivity of the samples deposited at 570 °C. These were explained by the increase of the dangling bonds sites and grain boundaries contribution;

iv) samples deposited at 620 °C and annealed have shown a smaller density of states assigned to dangling bonds and higher conductivity values in comparison with as-deposited samples. These were explained by the remove of the grain boundaries and by the increase of the crystalline phase.

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