

GROWTH AND CHARACTERISATION OF InGaAs(P) BY CBE TECHNIQUE

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Growth and evaluation of InGaAs(P) epilayers grown on InP by CBE technique for optical telecommunication applications is discussed. The grown InP epilayers have HALL mobility values of 70,000 and 2800 cm²/V.s with background impurities as low as 1×10^{14} cm⁻³ and 2×10^{15} cm⁻³ at 77 K and 300 K respectively. FWHM of the (004) Bragg reflection peak as narrow as 17 arcsec was obtained for these samples by HRXRD measurements. RT PL measurements also show typical spectra with a peak FWHM of about 19 nm. Lattice matched In_{0.53}Ga_{0.47}As was grown on InP and the strain value of 0.34 μ m thick layers was about 6.7×10^{-4} . The mobilities of the thick undoped ternary layer were 5970 (300 K) and 37,550 cm²/V.s (77 K) with carrier concentration in the range of 1.2×10^{15} – 4.2×10^{14} cm⁻³. Be-doped In_{0.53}Ga_{0.47}As layers with $p_{300K} = 9 \times 10^{18}$ cm⁻³ and $\mu_{300K} = 58$ cm²/V.s were also grown on InP which exhibits a line width (HRXRD) of nearly 25-30 arcsec. In_{1-x}Ga_xAs_yP_{1-y} quaternary epilayers (x = 0.24, y = 0.52) closely lattice matched to InP have also been grown. The HRXRD pattern of the quaternary layers shows a lattice mismatch of 2.4×10^{-5} and a luminescence peak FWHM of 8 meV. Further, the homogeneity of these layers was checked using FTPL study at different positions of the full wafer and it was extremely good. MQWs structures were also grown for the fabrication of SOA devices and are characterised by PL, absorption, ECV measurements.

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1. Introduction

In the last decade, development of growth technologies has been the main factor driving the advancement of III-V semiconductor electronic and opto-electronic devices. Today, epitaxial growth technologies can be classified into two main types: the ultra high vacuum techniques (molecular beam epitaxy (MBE), gas source MBE (GS-MBE), metalorganic MBE (MOMBE), and chemical beam epitaxy (CBE)) and the vapour phase techniques (vapour phase epitaxy (VPE), hydride-VPE, chloride-VPE, metalorganic VPE (MOVPE) or metalorganic chemical vapour deposition (MOCVD)). The choice of a technology clearly depends on its ability not only to fulfil material requirements but also economic criteria such as wafer cost, process yield, reliability, etc. At present time, MBE is the main technology used in the commercial production of microwave devices while MOVPE is more confined in the optoelectronic field. Out of many epitaxial techniques, the CBE technology is relatively a new technology and it has by now reached a mature level of development and is presently able to compete with the more established MBE and MOVPE technologies. Semiconductor markets based on microelectronic and optoelectronic devices are growing and expanding very quickly, leading the epi-wafer manufacturers to quest for reducing costs while device performance demands are increasing. Consequently, the number and the size of the wafer capability of the growth reactors are increasing. To reduce the cost, one of the possible ways is to increase the volume produced. However, the technological constraints associated with the large volume reactors development are often quite critical. In the case of MBE, the uniformity specifications imply the use of larger effusion cells and longer source/substrate distances, thus increasing the size of the machines and setting important problems such as reduced flux intensity, stability and thermal dissipation. On the other

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hand, the main drawback associated with high volume multi-wafer MOVPE reactors is the huge quantities of gases needed, hence increasing significantly the cost and of course the safety constraints. The potential of scale-up of CBE technology is quite high. In addition, the high quality materials grown with extremely reproducible control of thickness, compositions and uniformities make CBE a low cost technology for production of semiconductor epi-wafers [1]. The choice of one or the other technology is guided by two important key parameters, namely the potential of scale up existing machines and the cost criteria. For these key parameters, CBE seems to possess significant advantages particularly over MBE.

Comparison of CBE technique with that of MBE technique: in the case of phosphorus containing alloys for e.g., gallium indium phosphide (GaInP), the inherent problem of group V source reloading remains for MBE. In addition, no data are available on the defect densities obtained on a thick phosphide ternary alloys. So, for high volume production of GaInP/GaAs devices, the CBE technology is needed where the source reloading problem is minimum. In MBE, beryllium for a concentration of $2 \times 10^{19} \text{ cm}^{-3}$ exhibits a dramatic redistribution during growth, limiting its use for heterojunction bipolar transistor (HBT) applications, as it needs a very high base doping levels. Carbon is preferred for HBTs due to its low diffusivity and thermal stability. Although, carbon doping in MBE has been used in research laboratories, it seems very difficult to implement it in production machines. Carbon incorporation efficiency in CBE is found to be close to unity and high quality carbon doping has already been demonstrated by the high mobilities obtained, even for doping levels up to $1 \times 10^{20} \text{ cm}^{-3}$ [1]. Uniformities on $3 \times 4''$ MBE production machines are reported to be less than 1-2% (mean deviation value) following manufacturer specifications. Impressive results on uniformities have reported from Fujitsu Labs [2] by $3 \times 4''$ multi wafer CBE machine of uniformities of 0.2% of standard deviation for the Al composition and 1.8% of thickness uniformity. The limitation of MBE in terms of defect density, which induces a low fabrication yield, prevents its development for low cost and large volume integrated circuits. The typical value in a production environment is ranging from 50 to 100 defects/ cm^2 . In the CBE process, the defect density was 10 to 50 defects/ cm^2 and is independent of the grown materials. It is interesting to note that the low defect densities are obtained even after exposure of the chamber to air and without any bake out of the machine. As for the material aspects, DC and RF performances of high electron mobility transistor (HEMT) and more particularly HBT devices are found equivalent for both MBE and CBE growth technologies, even though there are difficulties related to the purity of Al starting precursors for CBE. The cost of organo-metallic sources for CBE is slightly higher than that of elemental gallium, aluminium or indium for MBE. However, the cost of source reloading is significantly higher in MBE compared to CBE. Due to the continuous decrease of, the level of the material in the crucible and thermal instabilities, MBE needs to be calibrated frequently reducing then the up-time of the machine. As a consequence, the cost of an epi-layer device structure is strongly influenced by the calibrated runs. In CBE, the pressure control system permits a very high level of reliability and flux reproducibility. This aspect represents one of the main advantages of the CBE technology.

Comparison of CBE technique with that of MOVPE technique: there is no need for a carrier gas in CBE, unlike MOVPE technique. Moreover, the flow control in CBE has higher accuracy and reproducibility than in MOVPE. The vacuum environment of CBE technique allows the application of an in situ measurements, in situ processing and/or surface diagnostic tools in the growth chamber. In CBE, group III, V and dopant precursor molecules reach the wafer surface without parasitic gas phase reactions. Therefore a higher growth efficiency than MOVPE, particularly in extremely toxic group V hydrides. The material consumption in CBE is much lower (at least one tenth) than that of MOVPE and so the costs for purchase, storage and waste management of toxic materials are drastically reduced. Thus, CBE is a much more environmentally beneficial technology. These economical, ecological and safety aspects deliver strong arguments for the use of CBE in an industrial environment [3]. With CBE, in situ etching is possible. An immediate switching between growth and etching can also be achieved, thus this process is compatible with selective area epitaxy or selective area processing such as in-situ etching, vacuum lithography. CBE is the preferred technology for selective area epitaxy for device applications, as it offers true selectivity, a lack of thickness and compositional variations.

Indium phosphide (InP) and phosphorous (P) based III-V alloys are important material systems for modern electronics, photonic and advanced devices applications [4]. Epitaxial

In_{1-x}Ga_xAs_yP_{1-y} compound semiconductors, lattice matched to InP substrates are basic materials for laser structures, which emit at the wavelength (λ) from 1.1 to 1.65 μm . Epitaxial growth of lattice matched and strained hetero-structures by CBE technique has become important [5, 6] and is receiving a great deal of attention in terms of understanding the growth phenomena and also in terms of the development of high-performance, novel electronic and opto-electronic devices. In this work, we discuss the growth and evaluation of InGaAs(P) epilayers and related semiconductor optical amplifier (SOA) structures grown on InP by CBE technique for optical telecommunication applications. High quality materials, including strained-layer quantum well structures for a wavelength of 1.55 μm (where the loss is minimum for fibre optic communication applications) has been grown and the good quality of the materials were ascertained by various characterisation techniques. Planar monolithic opt-electronic integrated circuits and photonic integrated circuits are becoming increasingly important in the development of low-cost components for optical telecommunication and optical processing systems. A key to the realisation of this integration is the ability to localise and integrate various devices namely lasers, detectors, wave guides, transistors, amplifiers etc. High speed performance of these devices is mainly dependent on the precise control of doping, thickness and composition. Usually such devices consist of layers of different materials with different doping concentrations. In this paper, the doping profile of a complete device structure of SOA device evaluated by ECV measurements is also presented.

2. Experimental

The epitaxial growth was carried out on VG80H MBE system equipped with a homemade gas handling system at Centro Studi e Laboratori Telecomunicazioni (CSELT), Torino, Italy. The schematic diagram of the CBE growth chamber is shown in Fig. 1 and furthermore details of the growth apparatus have been described elsewhere [7-10]. In the hydride lines, the pressure was controlled by solenoid valves while in the metalorganic lines the pressure was regulated by Granville-Phillips valves. The V/III ratio was monitored by means of an alternative procedure with respect to conventional ionisation methods. Every hydride line of known volume has a dedicated reservoir. The closure of the solenoid valve induced a pressure depletion, in the downstream line, measured by the control Baratron head. The amount of molecules injected into the chamber through the cracker cell was directly derived from the ideal gas law. The linearity of the regime was ensured, since only small variations from the set-point value were noticed, of the order of 2% for typical pressure values of 500 Torr. The same procedure was applied in order to control the pressure in the metalorganic lines. A dedicated reservoir with a 10 Torr Baratron head was used as the source of molecules. The working pressure was regulated by the thermostatic bath temperature containing the group III bottles, while the regulation values were set in the feedback configuration. By providing a good temperature stabilisation of the gas handling system, a direct measure of the number of injected molecules was obtained, thus avoiding the problems correlated to the aging of the ionisation gauge and to the uncertainties of ionisation coefficients. The deposition chamber is devoted to the realisation of quantum photonic devices and the range of grown materials covers the whole spectrum of InGaAs(P) compounds.

High purity hydrides, arsine (AsH₃) and phosphine (PH₃) are injected into a high-pressure cracker cell held at a constant temperature of 1173 K and the group V species (As, P) were thermally cracked. The metalorganic precursors used are trimethylindium (TMIn), triethylgallium (TEGa) for group III sources. The bubbler temperatures were 313 and 300 K respectively. All the precursors are introduced without the use of carrier gas. Beryllium was used for p-type doping whereas silicon was used for n-type doping and all the doping sources were in elemental (solid) form. The growth temperature is monitored by a thermocouple and double-checked with an optical pyrometer periodically calibrated against the melting point (800 K) of indium antimonide (InSb). The samples were mounted on molybdenum (Mo) blocks with indium bonding and the usual growth pressure is typically in the 10⁻⁵ mbar range. Before growth, a thermal cleaning procedure at 803 K for 5 minutes under the phosphine overpressure was adopted to completely desorb the surface native oxides on the substrate. Good quality epilayers were grown on an epi-ready, exactly oriented (001) InP substrates and the InP epilayer growth has been performed with a growth rate of 1 $\mu\text{m/h}$ at a temperature of

783 K. In the case of lattice matched InGaAs and InGaAsP, the growth rate was 0.65 $\mu\text{m/h}$ and 0.67 $\mu\text{m/h}$ respectively at the growth temperature of 798 K. MQWs were grown also at 798 K for the realisation of SOA.

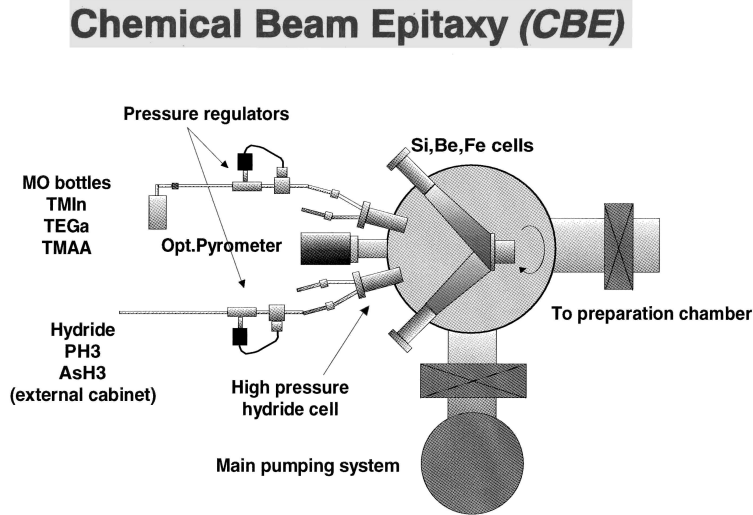


Fig. 1. Schematic diagram of the CBE growth system.

The electrical properties of the epilayers were characterised by performing HALL effect measurements using van der Pauw method. The applied magnetic field and sample current were normally 5 kG and 10 μA , respectively. The room temperature PL measurements were performed using the SCAT IMAGEUR system (Scantek, France). The excitation source used for all the measurements was 10 mW Helium-Neon laser (632.8 nm) with necessary filters. The emitted radiation was collected by the InGaAs photo detector and was analysed by the computer software (PLSCAN). Fourier transform PL (FTPL) measurements were also performed. The strain in the epilayers was estimated by high resolution X-ray diffraction (HRXRD) measurements. For the HRXRD measurements, four crystal diffractometer (Philips) was employed and experimental data were compared with a theoretical simulation software. It may be worthwhile to mention that all the results presented in this paper does not mean the best ever results obtained by CSELT, but they only shows the results of the growth runs performed during the stay of the author at CSELT.

Electrochemical capacitance-voltage (ECV) profiling on a test SOA device structure was carried out using Bio-Rad (PN4200) semiconductor profiler. Both the formation of the barrier and the removal of the material electrolytically have been carried out in an electrochemical cell and controlled electronically using the automatic equipment. For the semiconducting layers on conducting substrates, back contact configuration was used whereas front contact configuration should be employed for the layers grown on semi-insulating substrates. There were three electrodes employed other than the semiconductor (working) electrode. They are platinum (Pt) electrode for C-V measurements, carbon (counter) electrode for etching and saturated calomel electrode (SCE) as a reference electrode against which the equilibrium and over potential has been measured. The C-V behaviour is monitored using the auxiliary Pt electrode near the semiconductor surface to minimise the electrolyte series resistance. Dissolution was achieved by passing a current from the carbon cathode to the sample as anode, and this current was controlled to maintain a constant anodic potential with respect to the SCE reference electrode. All the potentials were measured with respect to the SCE (reference electrode) and the measurements have been carried out at room temperature. The etching and measurement potentials were normally selected such that they are smaller than the breakdown voltage of the electrolyte/semiconductor and this avoids any depth error if there is a leakage current. The materials can be readily profiled without any surface treatment or making an alloyed ohmic contact. 0.5M HCl acid solution was used as an electrolyte, which forms a good metal like contact (Schottky contact)

with the semiconductor. The electro-chemically etched surface was observed using Normarski microscope and the etched thickness was verified using a Tencor stylus profiler. The measured ECV carrier concentration values were compared with that of HALL effect values.

3. Results and discussion

3.1 Indium phosphide layers

For the HALL measurements, 2 μm thick InP epilayers were grown on InP:Fe substrate. From the HALL measurements (Table 1), it is evaluated that the grown samples have mobility values of 70.000 and 2.800 $\text{cm}^2/\text{V.s}$, with background impurities as low as $1.0 \times 10^{14} \text{ cm}^{-3}$ and $2.0 \times 10^{15} \text{ cm}^{-3}$ at 77 K and 300 K respectively. Full widths at half-maximum intensity of the (004) Bragg reflection peak as narrow as 17 arc sec (Fig. 2) for $\approx 2 \mu\text{m}$ thick layer was obtained by HRXRD measurements. Further, the room temperature PL measurements also show that the peak corresponds to the band gap of the material (1.349 eV) with FWHM of about 19 nm (Fig. 3). It was thus demonstrated that good quality InP layers have been grown by CBE.

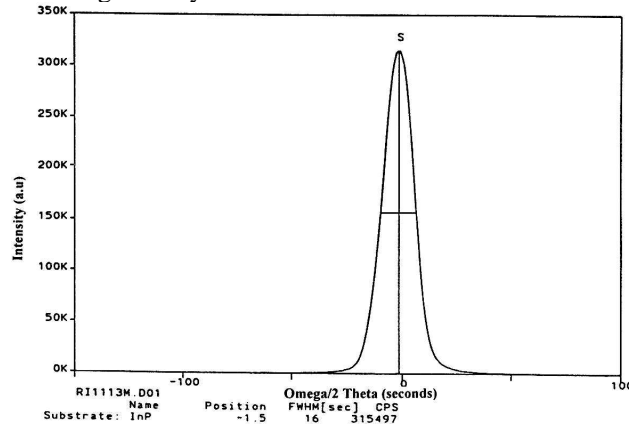


Fig. 2. HRXRD pattern obtained on the InP epilayer grown on an InP substrate.

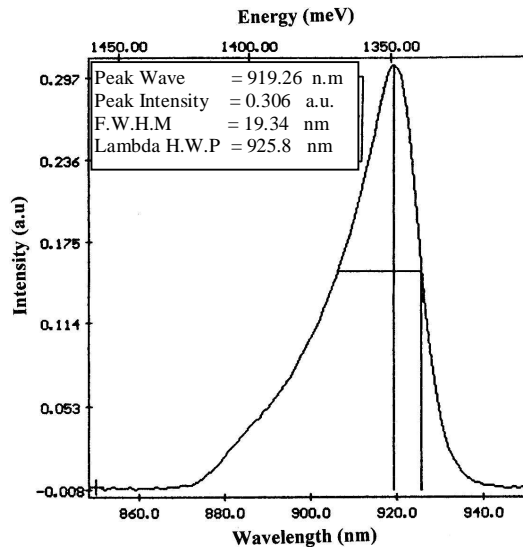


Fig. 3. Room temperature PL spectrum of an epilayer with a thickness of 2 μm having band-gap wavelength at 919 nm.

3.2 Indium gallium arsenide ternary layers

$\text{In}_x\text{Ga}_{1-x}\text{As}$ lattice matched ($x = 0.53$) to InP has emerged as a very important semiconductor material. High electron mobility and peak velocity are attractive for ultra-high speed devices. The band gap of 0.74 eV (1.65 μm) is ideal for photo-detectors in optical communication systems in the optimum wavelength range of 1.3 – 1.6 μm . Fig. 4 shows the HRXRD pattern of lattice matched $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer of thickness 0.34 μm grown on InP substrate with a strain value of 6.7×10^{-4} and the room temperature PL spectrum shows the band to band transition peak at a wavelength of 1.65 μm (Fig. 5). HALL measurements of 2.5 μm thick epilayers grown directly on InP:Fe substrates have mobilities of 5970 and 37.550 $\text{cm}^2/\text{V.s}$ at 300 and 77 K with carrier concentration (n) in the range of $1.2 \times 10^{15} - 4.2 \times 10^{14} \text{ cm}^{-3}$. Be doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layers with $p_{300\text{K}} = 9 \times 10^{18} \text{ cm}^{-3}$ and $\mu_{300\text{K}} = 58 \text{ cm}^2/\text{V.s}$ were also grown on InP, which exhibits a line width (HRXRD) of nearly 25-30 arcsec (Fig. 6).

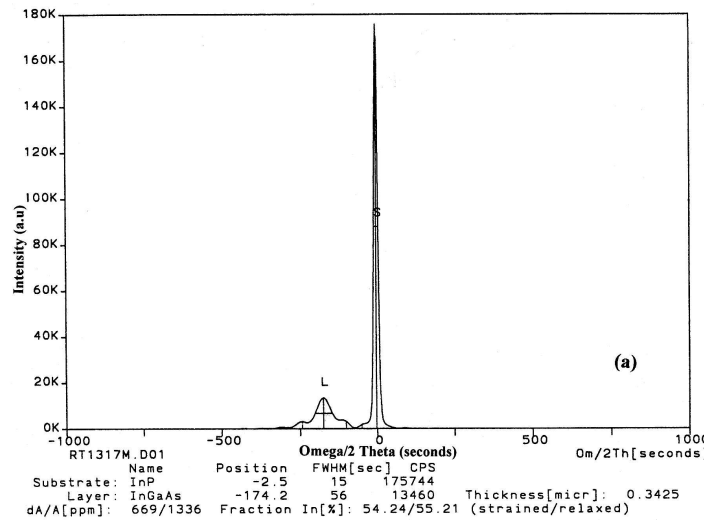


Fig. 4. HRXRD pattern of lattice matched $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer grown on an InP substrate.

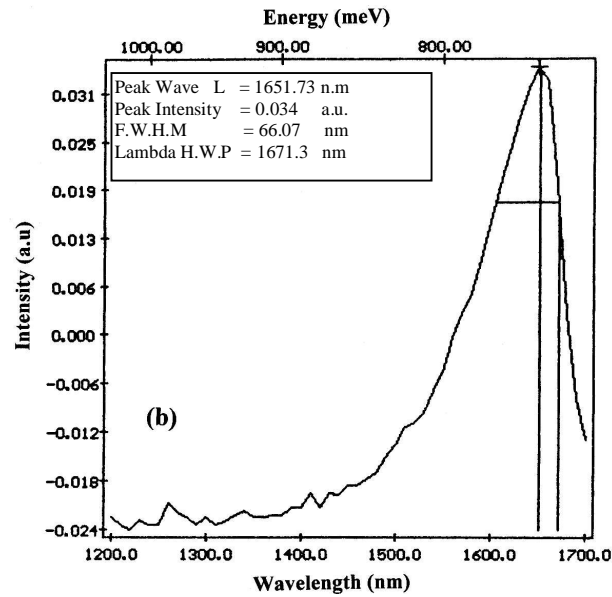
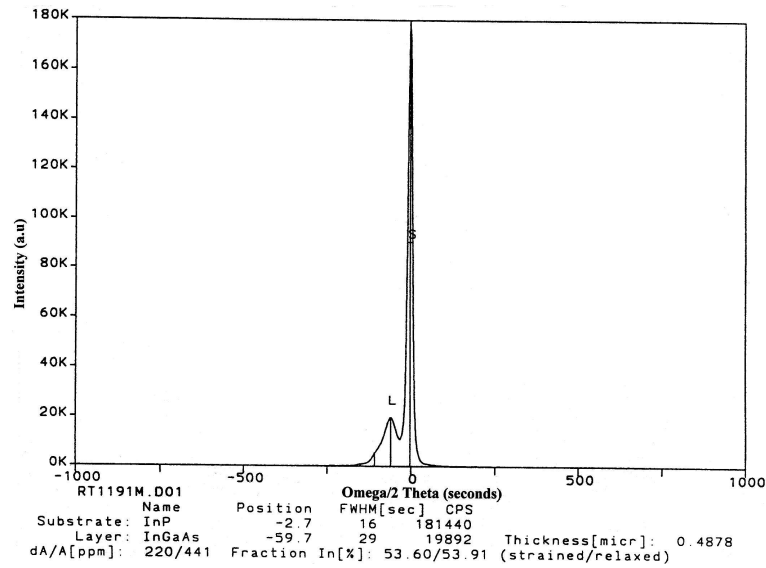


Fig. 5. Room temperature PL spectrum of the lattice matched $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ epilayer.

Table 1. Hall effect measurements of the CBE grown InP epilayers.

Sample No.	Growth temperature (T_g) K	At room temperature (300 K)		At 77 K	
		Carrier concentration cm^{-3}	Mobility $\text{cm}^2/\text{V.s}$	Carrier concentration cm^{-3}	Mobility $\text{cm}^2/\text{V.s}$
I1110	783	7.0×10^{16}	700	1.2×10^{16}	10.000
I1112	783	1.6×10^{16}	1190	2.0×10^{15}	23.000
I1113	783	2.0×10^{15}	2800	1.0×10^{14}	70.000
I1134	781	9.0×10^{16}	560	1.5×10^{16}	50.000
I1135	785	3.4×10^{16}	1840	1.1×10^{16}	12.600
I1136	780	5.0×10^{16}	1260	1.1×10^{14}	11.800
I1137	759	2.1×10^{17}	864	6.5×10^{16}	3.000
I1138	791	2.0×10^{15}	3075	1.0×10^{15}	54.500
I1143	784	7.2×10^{15}	2435	2.3×10^{15}	31.560

Fig. 6. HRXRD profiles of beryllium doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer ($p_{300\text{K}} = 9 \times 10^{18} \text{ cm}^{-3}$ and $\mu_{300\text{K}} = 58 \text{ cm}^2/\text{V.s}$).

3.3 Indium gallium arsenide phosphide quaternary layers

$\text{In}_{1-x}\text{Ga}_x\text{As}_y\text{P}_{1-y}$ quaternary epilayers ($x = 0.24$, $y = 0.52$) closely lattice matched to InP have also been grown. Fig. 7 presents the HRXRD pattern of $\text{In}_{0.63}\text{Ga}_{0.37}\text{As}_{0.87}\text{P}_{0.13}$ ($Q(\lambda=1.55\mu\text{m})$) with $\Delta a/a \approx 2.4 \times 10^{-3}$ and its room temperature PL spectrum is shown in Fig. 8. Note the appearance of the so-called Pendel-Lösungen fringes demonstrating the crystal perfection (Fig. 7). The homogeneity of the quaternary layers ($\text{In}_{0.72}\text{Ga}_{0.28}\text{As}_{0.57}\text{P}_{0.43}$) was also checked using FTPL measurements by taking spectra at three different positions of the wafer.

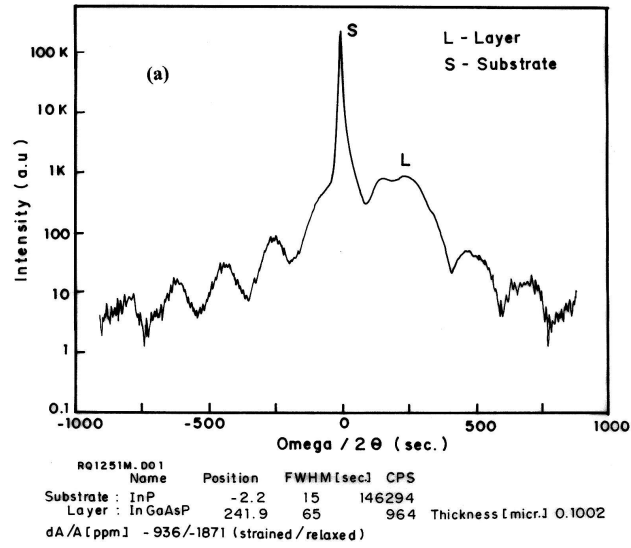


Fig. 7. HRXRD pattern of the closely lattice matched $\text{In}_{0.63}\text{Ga}_{0.37}\text{As}_{0.87}\text{P}_{0.13}$ ($\lambda = 1.55 \mu\text{m}$) to InP.

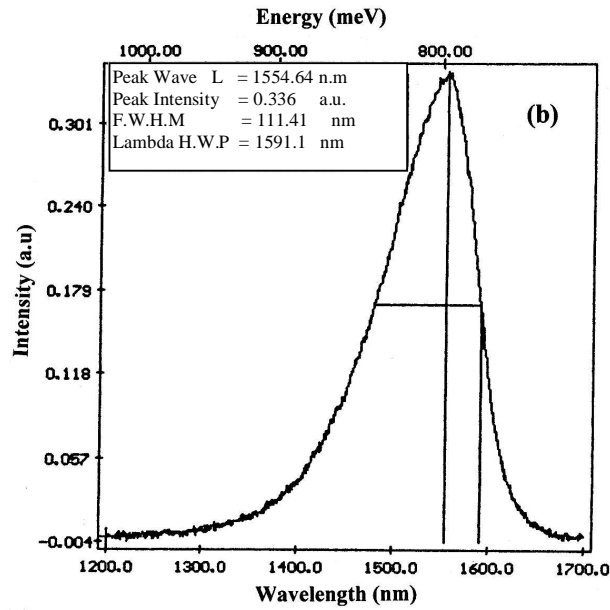


Fig. 8. Room temperature PL spectrum of closely lattice matched $\text{In}_{0.63}\text{Ga}_{0.37}\text{As}_{0.87}\text{P}_{0.13}$ layer.

The above sample with $\lambda_{\text{emission}} = 1.24 \mu\text{m}$ was typically grown at the temperature of 773 – 783 K with a growth rate of 0.85 $\mu\text{m/h}$. The arsenic flux (ϕ_{As}) was 0.61×10^{18} mol/sec and phosphine flux (ϕ_{P}) was about 3.4×10^{18} mol/sec. It was found that the homogeneity across the wafer was extremely good (Fig. 9). Further, the LT (4 K) PL measurement of the InGaAsP ($\lambda = 1.55 \mu\text{m}$) and InGaAsP ($\lambda = 1.24 \mu\text{m}$) shows a FWHM of 8 meV for both the samples, confirming the good quality of the epilayers.

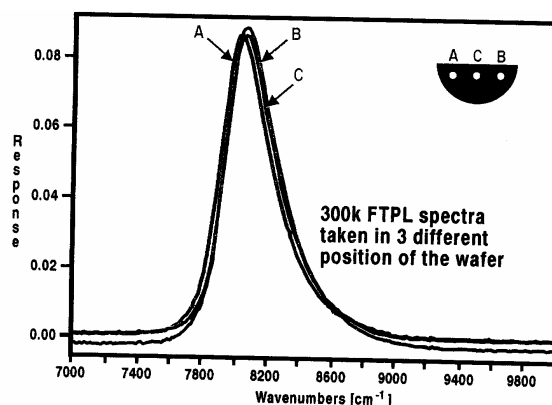


Fig. 9. Room temperature Fourier transform PL measurement performed on the $\text{In}_{0.72}\text{Ga}_{0.28}\text{As}_{0.57}\text{P}_{0.43}$ ($\lambda = 1.24 \mu\text{m}$) quaternary sample at three different position along the diameter of the wafer.

3.4 Multi quantum well (MQW) structures and semiconductor optical amplifiers

InGaAs/InP multi quantum wells, each well of thickness 7 nm, of 60 periods were grown. For MQWs, very intense luminescence peak with line width (FWHM) as low as 4.5 meV was obtained (Fig. 10) by 4 K PL measurements. The room temperature absorption spectra of the InGaAs/InP MQWs show a very sharp peak (Fig. 11). These studies show that the quality of the QWs was good with smooth and abrupt (“Squareness” of the QW) interfaces, few background impurities and a high PL efficiency. Semiconductor optical amplifiers are devices in which, the light once generated would not only be transmitted optically, but would also be amplified optically and received by direct optical detection. SOAs in conjunction with fiber amplifiers, will be used in future optical communications systems [11]. In addition, SOAs are promising devices for the potential coherent optical transmission system, because of their capability to preserve the coherence of light in frequency-modulated and phase-modulated signals. Furthermore owing to their miniature size, SOAs can be integrated monolithically with other optical circuits, opening the way to the eventual development of optical data processing. SOAs are also important for photonic integration for applications such as extended cavity lasers, wavelength dispersive medium (WDM) components, optical switching and others. For optical signal processing applications, MQW SOAs have many advantages, including high saturation output power, fast gain recovery time, wide gain bandwidth and ease of integrability in photonic integrated circuits [12].

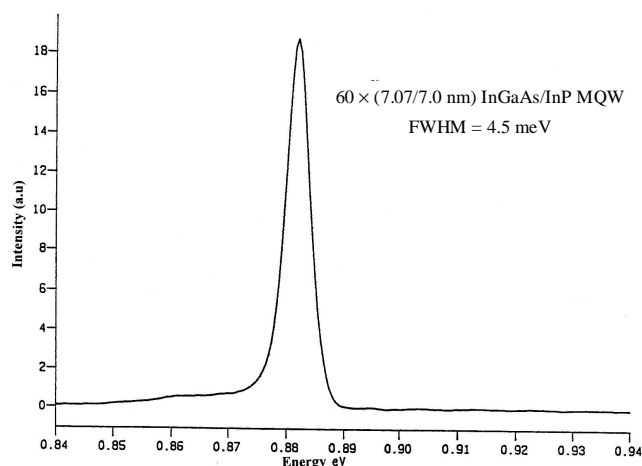


Fig. 10. Low temperature (4 K) PL spectrum of InGaAs/InP (7.0 / 7.0 nm, 60 periods) MQW structures.

A semiconductor optical amplifier can be identical in structure to a light emitting diode (LED) and a semiconductor laser. In many cases the same diode can behave sequentially as an LED, an amplifier and a laser depending on the magnitude of the injection current with which it is biased. In these cases, the diode consists of a sandwich of two or more types of semiconductors doped with impurities to have different electrical properties. At each end there is a cleaved crystal facet; the two end facets together act as plane-parallel, partially reflective mirrors. When an electric current is applied across the diode, valence electrons in the crystal lattice leave their places and move through the material, leaving behind “holes” in their places that other electrons can fill. When electrons and holes recombine in an active region bordered by junctions of the semiconductor materials, they spontaneously emit radiation at a wavelength determined by the material’s band gap – essentially the difference in energy between the electrons and the holes.

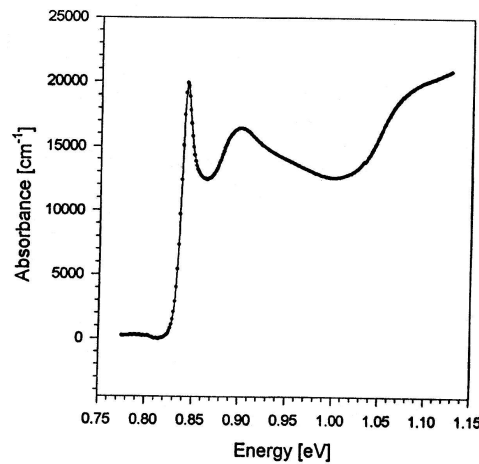


Fig. 11. Room temperature absorption spectra of an InGaAs/InP MQWs.

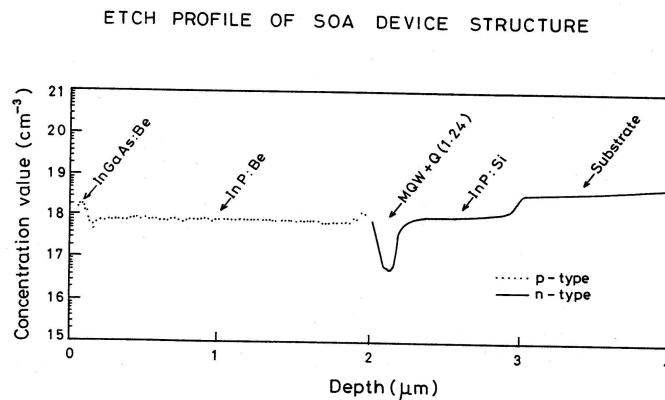


Fig. 12. Carrier concentration profile of a complete test device structure (SOA) grown by CBE technique, where the solid and dotted lines of the profile indicate n-type and p-type dopant respectively.

If the current applied is relatively low, the active region of the device begins to glow with light spontaneously emitted over a broad spectrum of wavelengths; at this point it is an LED. Any light inserted into one end of the diode from an external source will be absorbed by the crystal. As the current is gradually increased, there comes a point at which the diode will turn transparent to the incoming radiation: light inserted into it from an external source will no longer be absorbed, but will pass through the diode and be emitted out at the other end. That transparency point marks the

threshold of amplification: the current at which the diode begins to act as an amplifier. At current levels above that amplification threshold, the diode has net gain, intensifying incident light; that gain will increase as the current is increased. In addition, the diode is still spontaneously emitting its own light and amplifying that spontaneous emission; this amplified spontaneous emission (ASE) has somewhat narrower spectrum than the LED emission and is the amplifier's principal source of noise. As the current to the diode amplifier is further increased, at some point intrinsic to the material the gain begins to saturate: a further change in input current no longer results in an appreciable change in output. However, if the diode has some feedback mechanism, such as partially reflective end mirrors, the gain will not saturate; instead, at a second threshold current the net gain exceeds the losses to transmission through the end facets, absorption of free carriers within the crystal, scattering, and other cavity losses. At this lasing threshold current, internally generated light will resonate back and forth between the two crystal-facet mirrors, stimulating further emission with each pass. A certain amount of the radiation will be transmitted through the end mirrors, escaping the crystal, to be emitted over a fairly narrow spectrum of wavelengths as laser light. Thus the diode has changed from an amplifier to a laser. SOAs have been studied not only for direct amplification of an optical signal, but also for use as optical switches, in which the optical signal is turned on and off by switching the injection current.

3.5 ECV profiling of a semiconductor optical amplifier device structure

ECV measurements have been performed on a complete test device structure of SOA in order to understand the problems associated with profiling of multi layers containing both p-type and n-type materials [13]. The ECV results of a complete dopant profiling of the SOA device structure is shown in Fig. 12. There are four stages in obtaining an ECV profile:

- i) to obtain an current - voltage (I-V) plot (with and without illumination), from which the quality of the ohmic contact, the best etching voltage (V_{etch}) for electrochemical dissolution and voltage range for the acquisition of C-V plot are extracted
- i) to obtain C-V and conductance-voltage (G-V) plots. From the C-V plot, the quality of the Schottky barrier formed, the selection of correct dc bias (V_{meas}) to obtain the reliable carrier concentration measurements and quality of the model circuit (as inferred by G-V measurements) are found out.
- ii) to measure the depletion profile to obtain near surface information of carriers and also to verify the breakdown voltage of the junction.
- iii) using the informations obtained above (i-iii), perform the etch profile.

The test device structure consists of ternary (InGaAs), quaternary (InGaAsP) III-V alloy compounds with both p-type and n-type layers. The influence of junction series resistance (p-n junctions, hetero junctions) on the profile determination is not fully understood [14] and hence conventional HCl electrolyte is employed in order to avoid any other complications. The structure of SOA had separate confinement heterostructures (SCHs) with MQW as an active layer. The basic structure of the device consists of a 0.15 μm thick InGaAs:Be ($2 \times 10^{18} \text{ cm}^{-3}$) p⁺ top contact layer and the active layer contains MQWs (3 periods, thickness 0.15 μm) and 0.17 μm thick quaternary InGaAsP ($\lambda=1.24 \mu\text{m}$, undoped) layer. The active and InGaAsP layers were cladded between 1.8 μm thick p⁺ InP:Be ($1.5 \times 10^{18} \text{ cm}^{-3}$) and 1 μm thick n⁺ InP:Si ($1.5 \times 10^{18} \text{ cm}^{-3}$) layers. The above device structure has been grown on <100> InP:S ($n \approx 4 \times 10^{18} \text{ cm}^{-3}$) substrate. The concentration values mentioned within the brackets are the values that were calibrated by separate individual growth runs, performed on a semi-insulating InP substrate using HALL effect measurements and also with ECV measurement. There are two basic steps involved in the ECV profiling. Under controlled conditions, first is the measurement of the differential capacitance of the Schottky barrier formed at the electrolyte/semiconductor interface to obtain the carrier concentrations and the second is the electrochemical anodic dissolution reaction that removes the material at a controlled rate. These steps have been continued by performing repetitive etch/measure cycle to profile the carrier concentration as a function of depth. In p-type material, the dissolution is effected by the flow of holes, which occurs with the barrier under forward bias. In n-type material the dissolution reaction is promoted by supply of holes under reverse bias, which are generated optically by uniform illumination with blue light and are strongly absorbed in the near surface region of the semiconductor. The dissolution rate is

typically 1 μm per hour. The thickness of the material removed is calculated by integrating the dissolution current and applying Faraday's law. The actual depth scale is determined by adding this to the local depletion depth calculated from the capacitance. During the profiling of the device structure, etching was stopped as soon as the junction was realised. At each junction, the corresponding material parameters were given and then the etching was continued for a complete profiling. The junction is realised by observing abnormality in the dissipation factor [D-factor, which is the inverse of quality factor (Q) of the model circuit of the electrolyte/semiconductor], flat band potential value, depletion width and also in the sharp drop-off of dissolution current. The small "bump" in the ECV profiling indicates the junctions and it shows the interface control of the grown epilayers. The measured concentration and thickness values of the epilayers were in very good agreement with that of the expected values of carrier concentration and thickness and the complete profiling as a whole is satisfactory. However, the MQWs structures were not well resolved. During the profiling of very thin multi layers, the effect of junctions series resistance on the profile measurements are not understood fully and further studies are needed for the well resolved MQWs profiling.

4. Conclusion

The new epitaxial growth technique, CBE has been reviewed. The features of CBE technique is compared with both MBE and MOVPE techniques. Growth of InP, InGaAs and InGaAsP alloys has been performed on InP substrate and are characterised by HALL, HRXRD, PL (both room temperature and low temperature), and FTPL measurements. InP epilayers with mobilities 70,000 $\text{cm}^2/\text{V.s}$ at 77 K with background impurities as low as $1 \times 10^{14} \text{ cm}^{-3}$ have been obtained. The FWHM value of the layers by HRXRD measurements is 17 arcsec, confirming the good quality of the InP epilayers. Lattice matched $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer has also been grown on InP substrate with a strain value of 6.7×10^{-4} and with RT PL band to band emission peak at 1.65 μm . The layer has mobilities ($\mu_{77\text{K}}$) 37,550 $\text{cm}^2/\text{V.s}$ with free carrier concentration of $n_{77\text{K}} = 4.2 \times 10^{14} \text{ cm}^{-3}$. Be doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layers with $p_{300\text{K}} = 9 \times 10^{18} \text{ cm}^{-3}$ and $\mu_{300\text{K}} = 58 \text{ cm}^2/\text{V.s}$ were also grown on InP which exhibits a line width (HRXRD) of nearly 25-30 arcsec. Homogeneous $\text{In}_{0.76}\text{Ga}_{0.24}\text{As}_{0.52}\text{P}_{0.48}$ quaternary epilayers very closely lattice matched to InP have been grown. InGaAsP epilayers with wavelength 1.55 μm and 1.24 μm exhibits FWHM value of 8 meV at 4 K PL measurements. MQWs structures (InGaAs/InP, 7.0/7.0 nm, 60 periods) were also grown for the fabrication of SOA devices and are characterised by PL, absorption, ECV measurements. The 4 K PL studies of MQWs display intense luminescence peak with a line width as narrow as of 4.5 meV and the RT absorption spectra of the MQWs are very sharp indicating the smooth and abrupt interfaces of the QWs with less background impurities. SOA device structure with emission wavelength of 1.55 μm has been grown for fibre optical telecommunication applications.

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