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FIELD EFFECT ASSISTED THERMALLY STIMULATED CURRENTS IN CdS THIN FILMS DEPOSITED ON SiO_2/Si SUBSTRATES

M. Lisca*, E. Pentia, G. Sarau, L. Pintilie, I. Pintilie, T. Botila

National Institute of Materials Physics, Bucharest-Magurele, P.O. Box MG-7, 76900, Romania

Field effect assisted Thermally Stimulated Currents (TSC) measurements were used to differentiate between electron and hole traps in CdS thin films deposited on SiO_2/Si substrate. The electrode configuration was designed as for a pseudo-MOS structure, with drain and source contacts on the CdS film surface and using the Si substrate as gate electrode. Electron or hole traps will be favored to fill-up depending on the polarity of the gate voltage applied during illumination at low temperatures. Collection of the thermally released electrons or holes in the drain circuit will depend also on the polarity of the gate voltage applied during heating at constant rate. Comparing the results with those obtained in case of CdS films deposited on glass, it is possible to differentiate between SiO_2/ CdS interface traps and bulk CdS ones.

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1. Introduction

The A_2B_6 (as CdS) and A_4B_6 (as PbS) compounds are well known as very good photoconductive materials for visible and infrared regions of electromagnetic spectra[1]. However, the dynamic behavior of the photoconductive cells based on CdS and PbS films is influenced by the defects acting as trapping levels in the band-gap[1,2]. One of the methods often employed to investigate trapping levels in semiconducting materials and structures is that of Thermally Stimulated Currents (TSC)[3]. On the other hand, efforts to improve the photo-response of PbS films were made in the last years by using the so-called field effect assisted photoconductivity [4,5]. It is straightforward to assume that preferential filling of electron or hole traps is possible if the field effect is used in TSC measurements. That could help in distinguish between the two types of traps, knowing that only by simple TSC measurements this is not possible.

In this paper we report about the usage of field effect assisted TSC for investigation of trapping levels in pseudo-MOS structures in which the PbS was replaced by CdS. CdS was preferred because has a larger band gap, thus there is a larger probability to find deep levels in the forbidden band. Here the term “deep level” is used in the sense of levels discharging at relatively high temperatures. It is shown that by using gate voltages of different polarities during trap filling at low temperatures or during heating at constant rate it is possible to extract further information about the type of traps and about their spatial location.

2. Experimental

The SiO_2 layer of about 150 nm was grown on single-crystalline n-type Si wafers, by oxidation at 850 ^oC in an atmosphere containing oxygen and water vapors. The CdS film was

* Corresponding author: lisca@alpha1.infim.ro

deposited by chemical bath deposition (CBD) method described elsewhere [6]. Reference sample were prepared also on glass substrates in the same deposition bath. The thickness of the CdS film was in all cases around 70 nm. In order to obtain the pseudo-MOS structure gold electrodes in a coplanar configuration were deposited on the CdS film surface. These are the source and drain contacts. The gate contact is aluminum deposited on the backside of the Si substrate. For TSC measurements the sample was mounted in a closed-cycle He cryostat previewed with quartz windows. Trap filling with light is possible in this way, using an incandescent lamp in conjunction with an Oriel SM257 monochromator. The current was measured with Keithley 6517 electrometer.

It is known that the field effect is very effective to modulate and to get amplification in the case of monopolar conductivity [7,8]. In TSC-method the measured currents are, in most of the cases, given only by electrons or only by holes (thermally freed from the traps during heating up the sample). For this reason we considered that using field effect assisted TSC we could distinguish between electron and hole traps in CdS films. To this aim we performed two kinds of measurements. Firstly, the structure has been cooled down to 30 K, in dark, with V_g = 0 V. After biasing the gate (V_g = +/-8 V), the structure was illuminated for 5 minutes with light above CdS band-gap and with no voltage applied on the drain. The light was switched off first, the gate bias was returned to zero, and V_d = +20 V was applied. The TSC was measured during heating at constant rate (0.18 K/sec).

Secondly, the structure has been cooled down, in dark, to about 30 K, with either V_g = -8 V or V_g = +8 V and V_d = +20 V in order to measure the dark current for both gate polarities. At low temperature V_g was set to zero and then the sample was illuminated for 5 minutes to fill the traps. The drain voltage was also zero during illumination. After switching off the light the gate has been biased with V_g = -8 V or V_g = +8 V, and the TSC was measured with V_d = +20 V.

3. Results and discussion

Normally, the CdS thin films obtained by CBD method have n-type conductivity, and this is also our case (proved by hot probe both on CdS deposited on glass and on SiO_2). The investigated CdS thin films are of high resistivity (GΩ/□), so the total depletion state or the total accumulation state could be very easily reached. In the case of our films the free carrier concentration is very low, and the depletion and accumulation can be achieved with very low gate voltages. In any case the available charge is not enough to screen the high values of the gate voltage, thus it is assumed that the carriers generated under illumination will also sense its influence and will behave accordingly. The pseudo-MOS structure on which the measurements were made, is presented in Fig. 1.

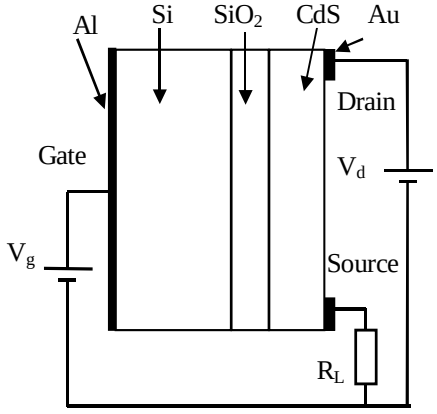

Fig. 1. Schematic of a pseudo-MOS CdS/SiO_2/Si structure together with the electric set-up used for photoconductivity measurements: V_d, drain voltage; V_g, gate voltage; and R_L, load resistance in the common source configuration.

The band diagrams with different gate voltages are shown as an insert in both Figs. 2 and 3 for TSC curves. When the sample is illuminated at low temperature under negative bias, then the hole

traps are favored to fill-up near the SiO_2/CdS interface and in CdS film volume because the electrons are swept out from the SiO_2/CdS interface and from the CdS too. Thus, the density of trapped electrons near the interface and in CdS film volume will be considerably diminished and the density of trapped holes will be increased. So, during heating up the TSC peaks due to the thermally freed holes must be accentuated while the TSC peaks due to the freed electrons must be diminished. When, at low temperature, the sample is illuminated under positive V_g the electron traps should be favored to fill-up near the SiO_2/CdS interface and in CdS film volume. Thus, during heating up the TSC peaks due to the thermally freed electrons must be accentuated and the TSC peaks for holes must be diminished. Looking to the shape of TSC curves obtained when the sample is illuminated under positive and negative bias, in Fig. 2 it can be seen that it is almost the same at higher temperature (over 250 K). The levels noted 1 and 2 are at the same position in temperature but are diminished for V_g = +8 V compared with V_g = -8 V. Only a deeper peak, noted with 3, seems to increase. The conclusion is that the peaks 1 and 2 are for holes and the peak 3 is for electrons. Comparing the TSC curves obtained for V_g = +8 V and for V_g = -8 V, applied during illumination at 25K, it can be observed that the shallow traps (under 250 K) are considerable reduced for positive bias applied on gate electrode. So it can be assumed that these are hole traps.

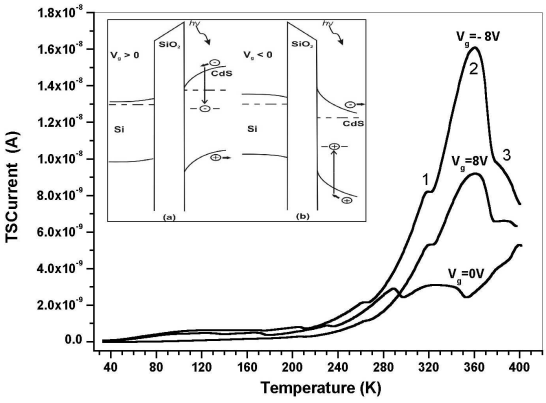

Fig. 2. Field effect assisted Thermally Stimulated drain-source Current in CdS/SiO_2/Si pseudo -MOS structure for negative and positive gate voltages applied only during illumination at 25K. Insert, energy-band diagrams for (a)V_g positive, (b) V_g negative.

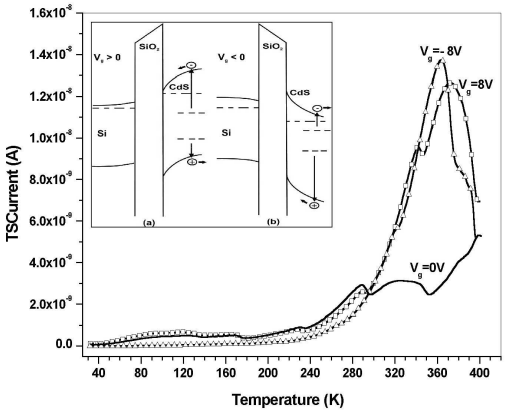

Fig. 3. Field effect assisted Thermally Stimulated drain-source Current in CdS/SiO_2/Si pseudo-MOS structure for negative and positive gate voltages applied only during heating up the structure. Insert, energy-band diagrams for (a)V_g positive, (b) V_g negative.

There will be no differences in trap filling when no gate voltage is applied during illumination, but the gate voltage applied during heating can separate the thermally released carriers. For positive V_g hole collection will be enhanced, while for negative V_g electrons will be collected more easily (Fig. 3). One can see from Fig. 2 and 3 that the TSC curve for V_g = -8 V from Fig. 2 is

very similar with TSC curve for V_g = +8 V from Fig. 3, and the same is valid for curve for V_g = +8 V from Fig. 2 and curve for V_g = -8 V from Fig. 3. These facts are consistent with assumption that the all peaks under 250 K are due to the traps for holes. The fact that in the high temperature region the magnitude of the TSCurrent is the same seems to support the assumption that the concentration of deep electron traps is about the same with that of deep hole traps.

The assumption that the shallow levels are located in the CdS volume and not near the SiO_2/CdS interface is supported by the fact that in the TSC curves obtained for CdS deposited on glass (Fig. 4) only these levels are observed and all deep levels (temperature higher than 200 K) are missing. So, it is clear that the deep levels (TSC peaks above 200 K in pseudo-MOS structures) are situated at the CdS/SiO_2 interface.

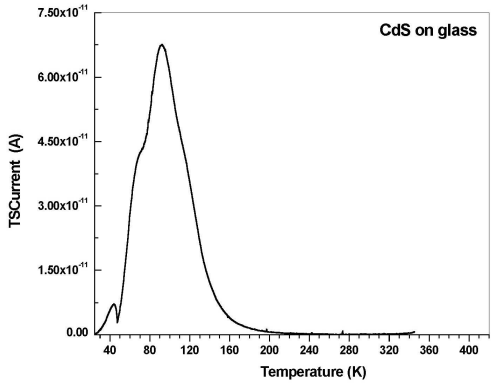

Fig. 4. TSC curve for CdS deposited on glass substrate (CdS on glass and on SiO_2 were deposited in the same chemical bath).

4. Conclusions

The field effect assisted TSC was applied on pseudo-MOS structures having the CdS film as conduction channel. Comparing the TSC curves obtained for different polarities of gate voltage it was possible to establish that the shallow levels are hole traps. At least two deep levels for holes (1 and 2) and one for electrons (3) were also observed by selective filling of traps. Comparing the TSC curves for CdS deposited on glass with those obtained in case of pseudo-MOS structures it was possible to establish that shallow levels are located more to the CdS film volume while the deep levels are located near the SiO_2/CdS interface. It was not the purpose of this paper to make quantitative evaluations, but only to signal that using the field effect during TSC measurements it is possible to extract more information about the type of traps and about their location.

Acknowledgement

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