

ON THE USE OF THE THERMAL STEP METHOD AS A TOOL FOR CHARACTERIZING THIN LAYERS AND STRUCTURES FOR MICRO AND NANO-ELECTRONICS

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This work concerns the use of the thermal step method (TSM) for measuring electric charge in metal-oxide-semiconductor (MOS) structures used in micro and nano-electronics. The TSM is a non destructive method for quantifying and localizing the electric charge in solid insulating materials and structures. Its principle is the application of a low thermal step to a short-circuited or dc-biased sample and the analysis of a current response, which depends on the charge present in the device. An adaptation of the technique (so far used in thick insulating materials and structures for electrical engineering) to short-circuited and biased MOS devices, is described. Results obtained on biased MOS structures and their correlation with classical capacitance-voltage (C-V) measurements are given. Estimations, by the TSM, of the amount of charge trapped in the oxide and of the space charge penetration depth in the silicon substrate are presented.

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1. Introduction

The metal-oxide-semiconductor (MOS) devices have become the fundamental components of modern electronics. Since 1970, the number of MOS devices integrated in a circuit has constantly increased by a factor of 4 every 3 years. This miniaturization and the increasing performance required for the microelectronic components impose more and more severe constraints to the insulator used in MOS devices, mainly silicon dioxide of thickness down to 1 nm. In such structures, the defects appearing during service and those inherent to the manufacturing process result in the formation of electric charges in the oxide layer, which may result, if not in a destruction of the device, at least in an alteration of its electrical properties leading to malfunction. For better understanding the breakdown and the shift of the threshold voltage of MOS transistors, it appears important to quantify and to localize the carriers. Methods like the capacitance-voltage technique (C-V) or the thermally stimulated discharge currents (TSDC) are currently used for detecting the charge in the oxide. Nevertheless, significant experimental problems have been encountered when using C-V on nanometric structures (where the leakage currents become important), and one may also ask if the entire amount of carriers are detected by C-V. The development of measurement methods able to bring further information is therefore of considerable interest.

The study of the impact of space charge on the insulating materials and structures for electrical engineering has been made possible by the set up, during the last twenty years, of non destructive measurement methods [1]. Most of them are based on the application of a non uniform stimulus (pressure or thermal) to the insulating device and on the recording of current or voltage responses, which depend on the amount and distribution of the accumulated charge. Among these techniques, the thermal step method (TSM) uses the propagation of a thermal wave within a short-circuited or biased insulating sample. The crossing of the thermal wave provokes a low and

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reversible electrical disequilibrium of the sample giving birth to a capacitive current, which allows to calculate the trapped charge and the internal electric field.

The TSM has been originally designed for thick dielectrics (25 μm to 20 mm [2-4]). However, the governing principle of the TSM allows to consider its application on lower thicknesses, as those of MOS devices used in micro and power electronics. The present paper deals with the application of the TSM on such structures. In the next section, the theoretical and experimental adaptation of the method for MOS characterization are treated. Results obtained on n and p -doped, biased and non biased devices, are then presented and discussed with respect to the corresponding C-V characteristics.

2. Experimental

MOS structure. To obtain a MOS device (Fig. 1), the surface of a semiconducting layer (silicon) is oxidized to form an insulating layer (SiO_2) of several dozens of nanometers. The top of the structure is constituted by a metal contact, also referred as the gate, and a second metal layer forms an Ohmic contact to the back of the semiconductor, also referred as the bulk or the source. The Si can be n or p -doped: the majority carriers in Si can be electrons or holes.

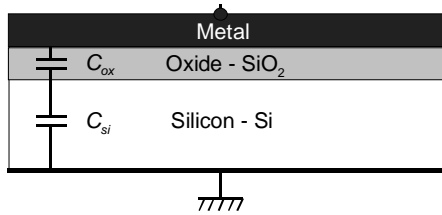


Fig. 1. Diagram of a MOS capacitance.

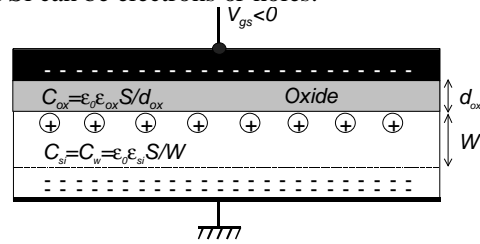


Fig. 2. MOS structure with n -type substrate in depletion mode.

Let us consider **an ideal MOS device with an n -doped substrate**, *i.e.*: (i) the semiconductor is doped so as its work function is equal to the work function of the metal, (ii) there are no interface states between the oxide and the Si substrate, and (iii) there is no space charge in the oxide. It comes out from Figure 1 that the MOS structure can be treated as a series of two capacitors, the capacitance of the oxide and the capacitance of the silicon: $1/C_{MOS} = 1/C_{ox} + 1/C_{Si}$. The capacitance of the oxide is independent from the applied voltage, $C_{ox} = \epsilon_0 \epsilon_{ox} S / d_{ox}$, with ϵ_0 the permittivity of the vacuum, ϵ_{ox} the dielectric constant of the oxide, S the surface of the metallic layer and d_{ox} the oxide thickness. The capacitance C_{Si} is determined by the appearance of a space charge layer W in the semiconductor under the effect of the voltage V_{gs} applied to the structure: $C_{Si} = \epsilon_0 \epsilon_{Si} S / W$, with ϵ_{Si} the dielectric constant of the silicon and W the thickness of the space charge layer, which is a function of V_{gs} .

There are three modes of operation of a MOS structure: accumulation, depletion and inversion. Under positive gate bias ($V_{gs} > 0$), the positive charge of the gate attracts electrons from the n -type substrate (majority carriers), yielding accumulation. The Si substrate behaves as a conductor: its capacitance is very high with respect to the SiO_2 capacitance, and consequently, in accumulation mode, the MOS capacitance is equal to the oxide capacitance: $C_{MOS} = C_{ox}$. When a negative voltage is applied ($V_{gs} < 0$), the negative charge of the gate pushes the electrons of the substrate away. A positive charge builds up in the semiconductor, due to the depletion of the semiconductor starting from the Si-SiO₂ interface (Fig. 2). The depletion layer width W further increases with decreasing gate voltage: the variation of the gate charge is compensated by a variation of W . In this mode (depletion), the capacitance of the structure is given by $1/C_{MOS} = 1/C_{ox} + 1/C_W(V_{gs})$. As the potential across the semiconductor continues to decrease ($V_{gs} \ll 0$), another type of charge emerges at the Si-SiO₂ interface: this charge is due to minority carriers (holes), which form a so-called inversion layer. As one further decreases the gate voltage, the depletion layer width W barely increases further since the charge in the inversion layer increases with the surface potential. The depletion layer width reaches therefore in inversion mode a maximum value W_{Max} , resulting in a minimum equivalent capacitance of the depletion layer C_{Wmin} . The value of C_{Wmin} is obviously $\epsilon_0 \epsilon_{Si} S / W_{Max} = C_{SiMin}$.

Consequently, when V_{gs} becomes lower than a threshold value V_{gsth} , the capacitance of the MOS structure remains approximately constant: $1/C_{MOS}=1/C_{ox}+1/C_{SiMin}$.

MOS structures with **p-type** substrates exhibits the same behaviour, the sign of V_{gs} being reverted.

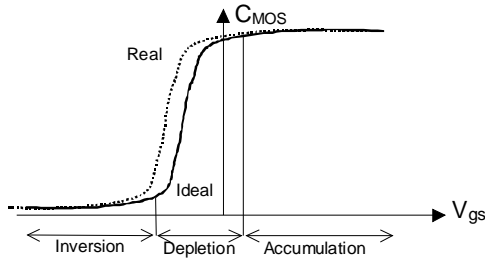


Fig. 3. Shape of C-V curves (n-type substrate).

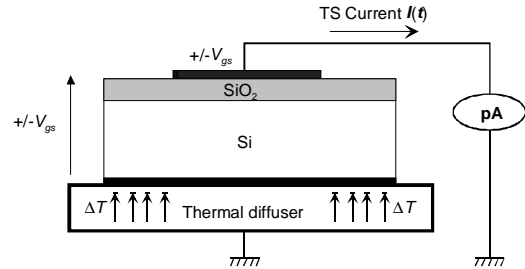


Fig. 4. Experimental set up for TSM on biased MOS.

The behavior described above is well-illustrated by C-V measurements, which are made by applying to the MOS structure high or low frequency sinusoidal voltages (1 kHz to 1 MHz) of several millivolts superposed to the bias voltage. The MOS capacitance is thus measured for different values of the bias voltage. For an ideal MOS capacitor with an **n**-doped substrate, the C-V curve has the shape from Fig. 3, where the three operating modes are put into evidence. However, as already asserted, **real MOS structures** often contain fixed and mobile charges in the SiO₂ layer and charge in surface states. The effect of these charges in C-V measurements is a stretching of the characteristics or a shift along the V_{gs} axis (Fig. 3). By using this curves one can calculate parameters such the doping level of the Si substrate, the oxide charge and the interface charge.

Principle of the TSM. The capacitive current generated by the redistribution of influence charges at electrodes as a consequence of applying a temperature step to a short-circuited insulating sample containing space charge, called thermal step (TS) current, is of the form [Refs]:

$$I(t) = -\alpha C \int_0^d E(x) \frac{\partial \Delta T(x,t)}{\partial t} dx \quad (1)$$

where d is the thickness of the sample, α is a constant related to the

variation of its capacitance C with temperature, $E(x)$ is the electric field distribution in the sample and $\Delta T(x,t)$ is the relative temperature distribution in the sample: $\Delta T(x,t)=T(x,t)-T_0$ (T_0 is the temperature of the specimen before applying the thermal step). Equation (1) can take a slightly different form if the analyzed specimen is not in short-circuit [3]. The temperature step is created in a heat exchanger adjoined to the measured sample, and the TS current measured with a current amplifier. If the temperature distribution is known, from (1) one can find the electric field and charge distributions.

Hypothesis and notations. The described principle can be applied to a micro or nanometric structure as a MOS capacitor (Fig. 4). The difference with respect to a classical TS measurement is that the MOS structure is composed of two layers with different electrical properties and behaviours, whilst a layer of a single dielectric material is measured in a classical experiment. The charges sensitive to the TS are the charge within the insulating SiO₂ (which is constant) and the charge forming the depletion layer in the Si substrate. The repartition and the amount of the latter vary considerably with respect to the mode of operation of the structure. Given the thickness of the oxide layer (≤ 100 nm) with respect to the thickness of the Si substrate ($> 100 \mu\text{m}$), it can be considered, in a first approach, that all the charges are concentrated at the Si-SiO₂ interface. We can then make the hypothesis of a space charge Q_0 present from the origin at the substrate/oxide border and varying in amplitude and in depth with the applied voltage. We will see that this macroscopic assumption, if does not allow for the moment to give the charge distribution within the structure at a nanometric scale, is sufficient to interpret and exploit the experimental results. The modeling is illustrated in Fig. 5, where Q_1 and Q_2 are the influence charges induced by Q_0 and d_{Si} the Si thickness (excluding the thickness of the charge layer in the substrate, for which we conserve the notation W). The oxide and the substrate are considered as homogenous, infinitely flat, of surface S (the electric field is assumed as constant in any plane parallel to electrodes) and placed at an initial temperature T_0 .

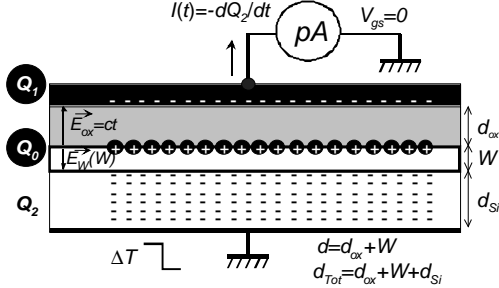


Fig. 5. Simplified model of an unbiased n -type MOS structure (space charge layer present from the origin at the Si-SiO₂ interface)

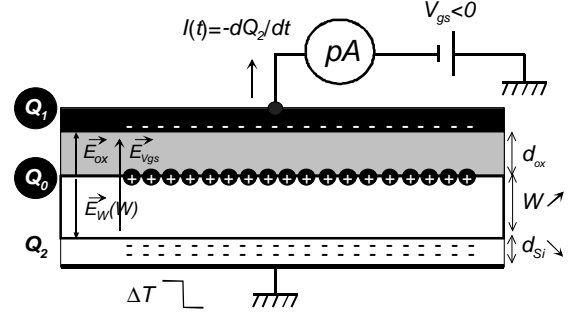


Fig. 6. Simplified model of a MOS structure with n -type substrate under negative bias

Expression of the TS current in short-circuit conditions. By using the electrostatic and thermal expansion equations, we can derive for the TS current in short-circuit conditions ($V_{gs}=0$) the expression:

$$I(t) = +Q_0 \frac{\alpha_{Si} d_{ox}}{\epsilon_{Si} \epsilon_{ox} \left(\frac{W}{\epsilon_{Si}} + \frac{d_{ox}}{\epsilon_{ox}} \right)^2} \int_0^{d_{Si}+W} \frac{\partial \Delta T(x,t)}{\partial t} dx_{Si} - Q_0 \frac{\alpha_{ox} W}{\epsilon_{Si} \epsilon_{ox} \left(\frac{W}{\epsilon_{Si}} + \frac{d_{ox}}{\epsilon_{ox}} \right)^2} \int_{d_{Si}+W}^d \frac{\partial \Delta T(x,t)}{\partial t} dx_{ox} \quad (2)$$

Hence, the TS current is a function of the amount of apparent interface charge Q_0 , of the Si and SiO₂ thermal variation parameters α_{Si} and α_{ox} and of the interface charge width W . The way of obtaining (2) is the same as the one presented in [3-4]. The temperature propagation across the structure (infinite semi-plane) obeys to the law:

$$\frac{\partial \Delta T(x,t)}{\partial t} = \Delta T \frac{x}{t} \sqrt{\frac{1}{D4\pi t}} \exp\left(-\frac{x^2}{4Dt}\right) \quad (3)$$

with D the thermal diffusivity of the sample. Given that the thickness of the MOS capacitor is much lower than the equivalent thickness x_0 [3-4] of the air layer between the thermal diffuser and the sample and of the copper top of the thermal diffuser (of the order of 1 mm), we can consider that the temperature within the structure depends only on time:

$$\frac{\partial \Delta T(x,t)}{\partial t} \approx \Delta T \frac{1}{t} \sqrt{\frac{\tau}{\pi t}} \exp\left(-\frac{\tau}{t}\right) \quad (4)$$

where $\tau = x_0^2/4D$. With the thermal parameters of Si and SiO₂ and given the bench configuration, we got $\tau = 0,484$ s. Expression (4) presents a maximum for $t_M = 2\tau/3$. The maximum of the TS current in short-circuit conditions is then given by:

$$I(t)_{Max} = -Q_0 \frac{(\alpha_{Si} - \alpha_{ox})(W \cdot d_{ox})}{\epsilon_{Si} \epsilon_{ox} \left(\frac{W}{\epsilon_{Si}} + \frac{d_{ox}}{\epsilon_{ox}} \right)^2} \left[\frac{\partial \Delta T(x,t)}{\partial t} \right]_{Max} \quad (5)$$

Expression of the TS current in a biased device. When a bias voltage V_{gs} is applied to the structure, a supplementary TS current $I_V(t)$ emerges:

$$I_V(t) = -\frac{V_{gs} S (\epsilon_{ox} \alpha_{Si} W + \epsilon_{Si} \alpha_{ox} d_{ox})}{\epsilon_{Si} \epsilon_{ox} \left(\frac{W}{\epsilon_{Si}} + \frac{d_{ox}}{\epsilon_{ox}} \right)^2} \left[\frac{\partial \Delta T(x,t)}{\partial t} \right] \quad (6)$$

The total TS current will then be the sum of (2) and (6), with a maximum of:

$$I(t)_{Max} = \left[\frac{\partial \Delta T(x,t)}{\partial t} \right]_{Max} \cdot \frac{-Q_0(\alpha_{Si} - \alpha_{ox})(Wd_{ox}) - V_{gs}S(\epsilon_{ox}\alpha_{Si}W + \epsilon_{Si}\alpha_{ox}d_{ox})}{\epsilon_{Si}\epsilon_{ox} \left(\frac{W}{\epsilon_{Si}} + \frac{d_{ox}}{\epsilon_{ox}} \right)^2} \quad (7)$$

In (7), W depends on applied potential V_{gs} . For example, in a n -type MOS capacitance with positive charge trapped in SiO_2 , W increases with decreasing V_{gs} and decreases with increasing V_{gs} (e.g. Fig. 7).

Samples and measurement conditions. The results presented below were obtained on MOS capacitors manufactured at the LAAS Technological Center in Toulouse, France. They were constituted of a Chrome gate (thickness: 200 nm, surface $S = 0.19 \text{ cm}^2$), of a SiO_2 layer $d_{ox}=100 \text{ nm}$, of a 10^{15} cm^{-3} n or p -doped Si substrate (thickness: 500 μm) and of an Aluminum-made back Ohmic contact of 500 nm. Thermal steps of $-30 \text{ }^\circ\text{C}$ and $+20 \text{ }^\circ\text{C}$ were applied to the specimens placed with the Si side onto the thermal diffuser (Fig. 4). During the measurements, dc voltages between $-5 \text{ }^\circ\text{V}$ and $+5 \text{ }^\circ\text{V}$ have been applied to the gate by mean of a bias circuit integrated in the current amplifier.

3. Results

Fig. 7 to 9 show the TS currents obtained on a n MOS capacitance submitted to a *negative* $-30 \text{ }^\circ\text{C}$ thermal step. The first measurement has been made in short-circuit conditions in order to test the structure before bias. The measurements performed in accumulation mode (positive bias, Fig. 7) show a low quasi-linear decrease of the TS currents as the bias voltage increases. After this series of measurements, we have verified by a short-circuit experiment that the initial state of the oxide was not modified (unchanged short-circuit TS current). The results obtained under negative bias (Fig. 8) show a significant decrease of the TS signal with the decrease of the negative bias voltage. Fig. 9 is a detail of the region corresponding to the beginning of the inversion area observed experimentally by C-V (Fig. 10). For $V_{gs}=-1.7 \text{ V}$, one can note the inversion of the TS signal. In contrast with the quasi-linearity noted for $V_{gs}>0$, we are here in the presence of a notably straighter variation of the signals. However, starting from -2 V , we note (Fig. 8) a re-augmentation of the TS currents, similarly to the positive bias region.

Fig. 11 to 16 show TS currents obtained with a *positive thermal step* of $20 \text{ }^\circ\text{C}$ on n and p MOS capacitances from another series of manufacturing. The advantage of using a low positive thermal step is to avoid the problems of condensation, which can affect the measurements. The behaviour of the n devices is the same of those presented in Fig. 7-9, except for the sign of the TS signals which is reverted (as the thermal step is of opposite sign) and of the value of the inversion voltage. The p capacitance exhibit signals of opposite polarity to the n one, in accordance with the change of sign of the majority carriers in the substrate.

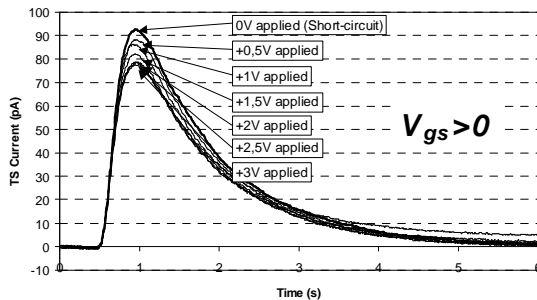


Fig. 7. TS currents obtained on a n MOS sample in accumulation mode ($V_{gs}>0$) with a TS of $-30 \text{ }^\circ\text{C}$.

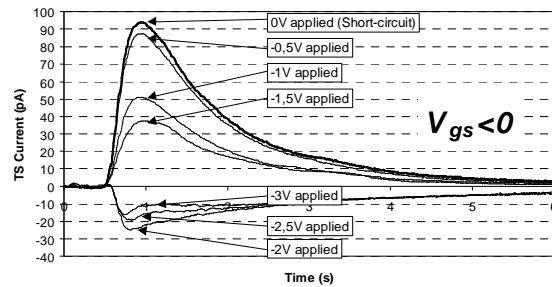


Fig. 8. TS currents obtained on a n MOS sample in depletion and inversion modes ($V_{gs}<0$) with a TS of $-30 \text{ }^\circ\text{C}$.

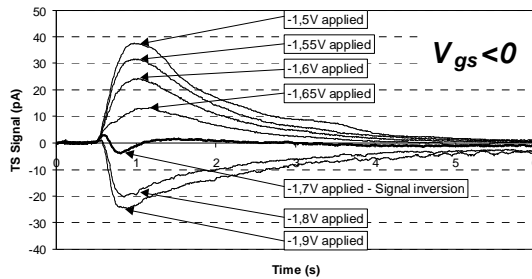


Fig. 9. TS currents obtained on an *n* MOS sample in inversion mode ($V_{gs} < 0$) with a TS of $-30\text{ }^\circ\text{C}$ (detail in the inversion region).

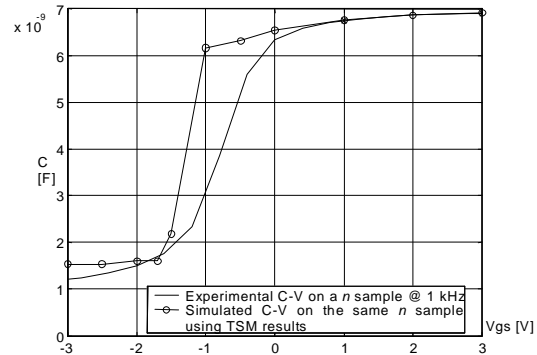


Fig. 10. Experimental C-V curve on a *n* MOS and C-V curve simulated using the values of the depletion layer width W derived from TS measurements.

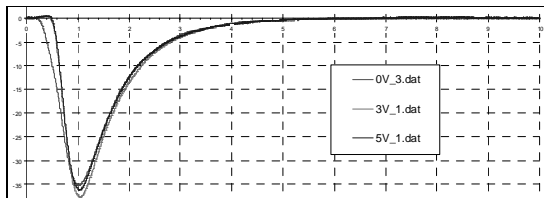


Fig. 11. TS currents on a *n* MOS sample in accumulation mode ($V_{gs} > 0$) (TS of $+20\text{ }^\circ\text{C}$).

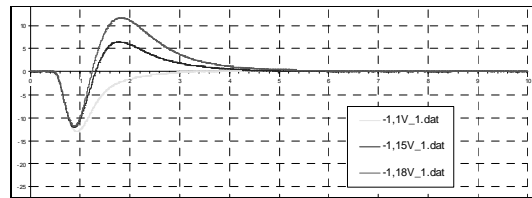


Fig. 12. TS currents on a *n* MOS sample in depletion mode ($V_{gs} < 0$) (TS of $+20\text{ }^\circ\text{C}$).

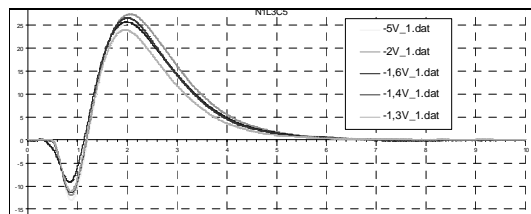


Fig. 13. TS currents on a *n* MOS sample in inversion mode ($V_{gs} < 0$) (TS of $+20\text{ }^\circ\text{C}$).

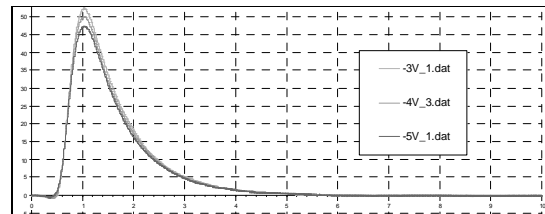


Fig. 14. TS currents on a *p* MOS sample in accumulation mode ($V_{gs} < 0$) (TS of $+20\text{ }^\circ\text{C}$).

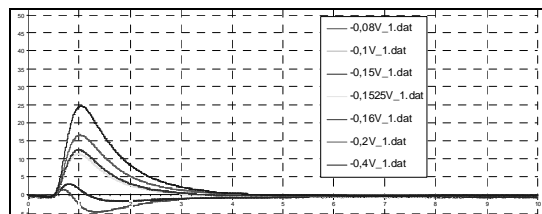


Fig. 15. TS currents on a *p* MOS sample in depletion mode ($V_{gs} > 0$) (TS of $+20\text{ }^\circ\text{C}$).

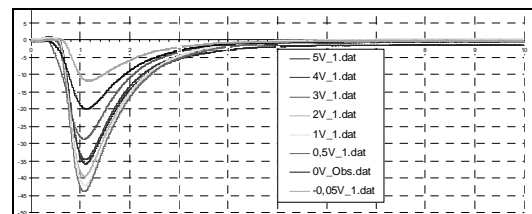


Fig. 16. TS currents on a *p* MOS sample in inversion mode ($V_{gs} > 0$) (TS of $+20\text{ }^\circ\text{C}$).

4. Discussion

Let us now interpret the results of the TS measurements on the basis of equation (7) and compare them to C-V results. If we consider the *n* MOS capacitance from Fig. 7 to 9, when the applied positive voltage increases ($V_{gs} > 0$: accumulation), the weight of the term $V_{gs}S$ also increases, but the space charge layer depth W (low with respect to the oxide thickness) decreases. The result is a decrease of the TS current, due to the decrease of W , which has a more important effect than the augmentation of $V_{gs}S$. This low decrease of the TS current under positive bias (Fig. 7)

is perfectly correlated with the feeble augmentation of the MOS capacitance observed by C-V (Fig. 10).

$V_{gs} < 0$: When the structure is biased negatively, the space charge width W increases significantly, and in the same time the weight of the V_{gs} term in (7) increases. Consequently, the TS current decreases in a much more significant manner than for positive biasing (Fig. 8). The zero TS current (observed for $V_{gs} = -1.7$ V on this n sample) corresponds to the quasi-equality of the Q_0 and V_{gs} terms in (7). The spreading of the space charge thickness W increases further with the decrease of the applied voltage until W reaches its maximum value $W = W_{Max}$, after which the structure switches to inversion mode. The significant decrease of the TS current is in good accordance with the important decrease of the MOS capacitance (by a factor of 7) observed by C-V (Fig. 10).

$V_{gs} \ll 0$: In this case (inversion mode, Fig. 8-9), the space charge width W barely varies ($W \approx W_{Max}$), the TS current variation being made essentially on the expense of the augmentation of the absolute value of V_{gs} and of the augmentation of Q_0 by minority carriers. The increase of Q_0 also changes the variation direction of the current: a low augmentation is observed. This increase can be correlated with the moderate decrease of the MOS capacitance observed in the inversion region by C-V.

This analysis is confirmed on the n MOS characterized with a positive thermal step. (The sign of the signals is changed because the thermal step sign is reverted). This analysis also holds for the p -type structure, where the polarity of the voltage is reverted (the majority carriers in the substrate are holes instead of electrons). The qualitative behavior of the n and p MOS capacitors derived from the TS measurements is in good agreement with the C-V characteristics.

Calculation of the charge and of the depletion layer width. Values of Q_0 and W calculated using equation (7) for the n -MOS sample from Fig. 7 to 9 are given in Table 2. They have been obtained by using the parameters presented in Table 1 (the values of α_{Si} and α_{ox} have been estimated theoretically).

Table 1. Parameters used in equation (7).

Parameter	Value
ϵ_{Si}	$12\epsilon_0$
ϵ_{ox}	$4\epsilon_0$
α_{Si}	10^{-2} K^{-1}
α_{ox}	$2 \cdot 10^{-4} \text{ K}^{-1}$
d_{ox}	100 nm
S	$19 \cdot 10^{-6} \text{ m}^2$

Table 2. Q_0 and W obtained from the TS currents.

Sample	n MOS (TS currents from Fig. 7-9)		
V_{gs} [V]	I_{Max} [pA]	Q_0 [C]	W [nm]
+3.00	+77	1.20E-8	1.3
+2.00	+78	1.20E-8	3.4
+1.00	+85	1.20E-8	8.0
+0.00	+91	1.20E-8	18.7
-0.50	+87	1.20E-8	29.7
-1.00	+52	1.20E-8	38.0
-1.50	+38	1.20E-8	650.0
-1.70	~ 0	1.20E-8	1000.0
-2.00	-25	1.32E-8	1000.0
-2.05	-	-	-
-2.50	-19	1.70E-8	1050.0
-3.00	-16	2.07E-8	1050.0

A theoretical calculation performed in flatband conditions for this n -MOS structure [5-6] gives at inversion a value for W of the order of 1000 nm, which is very close from that determined by TSM (Table 2, $V_{gs} = -1.7$ V). With the TS-calculated values of W , the C-V curve of the structure can be simulated. Such a simulation is shown in Fig. 10, where it is compared to the experimental C-V obtained on the same sample. A good agreement is observed between the two curves, but the TS-simulated C-V is shifted with respect to the experimental one. This shift may be due to the imperfection of the used model (it is very likely that not all the oxide charge is located at the interface), but can also be interpreted in terms of dynamics of measurements, *i.e.* the dynamics of TS measurements (~ 1 Hz) could reveal more space charge than that revealed by C-V characterizations, with much quicker dynamics (1 kHz).

To summarize, the simplified model used here seem to give satisfactory results for both positive and negative bias, with a good estimation of Q_0 and W . However, these quantities are derived using only the maximum of the thermal step current. There is more information to be drawn from the TS measurements, in particular near the inversion threshold, were the experimental current is not flat, as would predict equation (7). A thorough modeling could allow in the future an analysis of more than one TS signal data, *i.e.* to separate completely the effects of oxide charge from that of

the substrate charge and to calculate in a more precise manner the repartition of the charge in the structure.

5. Conclusions and prospects

The use of the thermal step method for measuring space charge in micro and nanoometric structures as biased MOS devices has been presented in this paper. An approach of the MOS structures by a simple electrostatic and thermal model allows to estimate without deconvolution the amount of charge trapped in the oxide and the space charge area width in the silicon substrate. The results obtained on *n* and *p* MOS show a good correlation, both qualitatively and quantitatively, between the classical capacitance-voltage measurements and the measurements performed by the thermal step method.

The analysis of the thermal step currents acquired under different bias voltages reveals easily the three operating modes of the MOS structures (accumulation, depletion and inversion). The signals given by the thermal step method allow to situate precisely (± 0.01 V) the inversion threshold.

A more detailed electrostatic modeling of the MOS device should allow to obtain a more precise distribution of the charge within the oxide and the semiconducting substrate. This could open the way to the set up of a characterization technique applicable directly to MOS components used in microelectronics.

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