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CHARACTERISTICS OF POLYSILICON TFTs, HYDROGENATED BY ION IMPLANTATION P-CHANNEL

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Self-aligned polycrystalline silicon thin film transistors (PS TFTs) with different phosphorus channel doping have been investigated by the conduction method. The polysilicon gate was heavily doped by ion implantation of phosphorus. The source and drain electrodes were heavily doped by ion implantation of boron. A gate oxide 45 nm thick was grown in dry oxygen. On a parallel series of wafers, the grain boundary and gate oxide interface states were passivated by ion implantation of hydrogen through the polysilicon gate. Fitting the experimental data for the threshold voltages and hole mobilities with the theory reveal that hydrogenation by ion implantation improves the performance of the TFTs. The results confirm that such hydrogenation is a promising technology for the improvement of the performance of PS TFTs.

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1. Introduction

Polysilicon thin film transistors (PS TFTs) are used in high performance active matrix liquid crystal displays (AMLCDs) as pixel and driver transistors for both p- and n- channel transistors, in high density static RAMs as pull up transistors (only p-channel), projectors, etc [1]. The characteristics of PS TFTs are strongly dependent on the grain boundary states in the channel polysilicon. The high density of grain boundary traps makes the electrical characteristics unsuitable for implementation in integrated circuits. Usually, hydrogenation by RF plasma or ion implantation of hydrogen is applied to decrease the density of the grain boundary traps [2]. Ion implantation of hydrogen is a promising technology for such hydrogenation, as can be implanted at the desired depth and concentration in the multilayered structure of a PS TFT.

In the present work, the influence of such implantation on the threshold voltages and hole mobilities in PS TFTs with different phosphorus channel doping levels is investigated.

2. Experimental details

In this study, PS TFTs were fabricated with a polysilicon layer nominal thickness of 220 nm. They were deposited on thermally oxidized silicon wafers by LPCVD using SiH_2 source gas at 620°C at a pressure ~ 0.4 Torr. The wafers were then thermally oxidized and annealed at 1000°C for 3 h in dry N_2 ambient, for grain enlargement. The polysilicon was phosphorus implanted at an energy of 35 keV and doses of 5.10^{11}, 10^{12} and 5.10^{12} cm^{-2}, through the thin SiO_2 layer. The oxide layer then was removed and SiO_2 with a thickness of 45 nm was grown at 1000 °C in dry oxygen as a gate dielectric for the PS TFTs. Transmission electron microscopy analysis showed that

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the polysilicon layers had a columnar structure with an average grain size about 100 nm. The final thickness of the polysilicon channel layer was ~ 150 nm. The 200 nm thick polysilicon gate electrode and the source and drain regions of the transistors were heavily doped by self-aligned boron ion implantation with a dose $>10^{15}$ cm^{-2} for p-channel devices. Then a 100 nm thick oxide layer was deposited by LPCVD as a cap layer. After opening the contact holes, Al/Si was deposited and patterned. The polysilicon was hydrogenated by ion implantation at a dose of 10^{16} cm^{-2} and an energy of 130 keV, through the top passivated oxide, the polysilicon gate and the gate oxide. Finally, the wafers were annealed at 450 °C for 30 min in a hydrogen ambient. PS TFTs with a channel width W = 50 µm and length L = 10 µm (L_{eff} = 6 µm) were fabricated. The cross section of a p-channel PS TFT, and the hydrogen distribution, are shown in Fig. 1. The transistor transfer characteristics were measured using a Keithley 617 Programmable Electrometer.

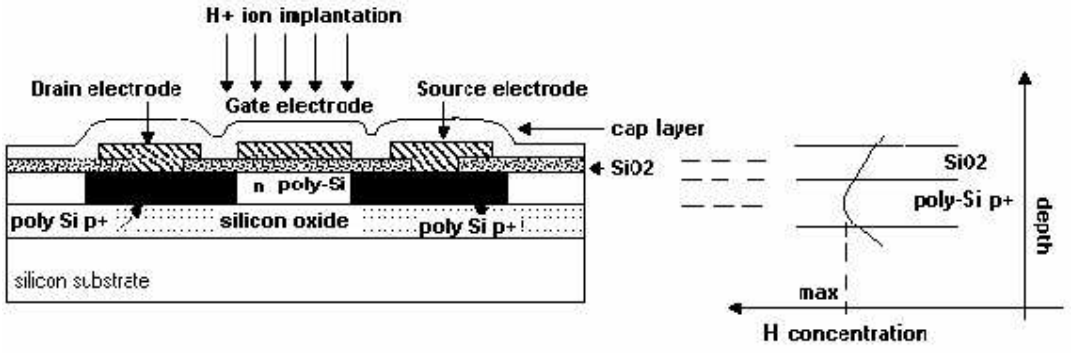

Fig. 1. Cross section of a polysilicon p-channel TFT.

3. Results and discussion

The transfer characteristics of PS TFTs with different levels of channel polysilicon doping in the sub-threshold and linear region at U_d = 0.5 V, for unhydrogenated and hydrogenated structures, are shown in Fig. 2 and Fig. 3, respectively.

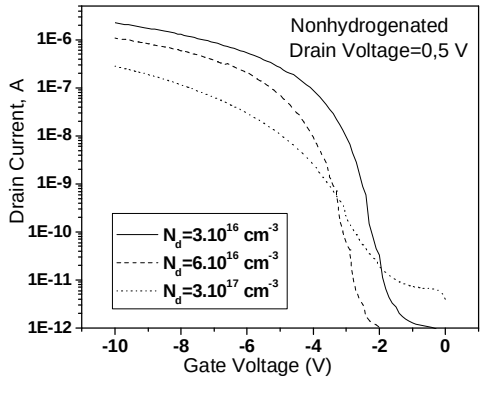

Fig. 2. Transfer characteristics of unhydrogenated TFTs with different channel doping levels.

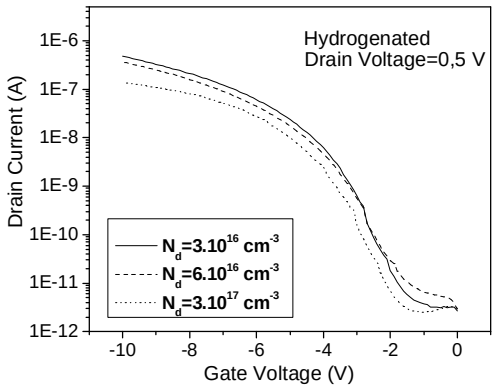

Fig. 3. Transfer characteristics of hydrogenated TFTs with different channel doping levels.

The threshold voltages were estimated by extrapolation of the linear part of the transfer characteristics onto the gate voltage axis. The values for unhydrogenated TFTs were found to be higher than those for hydrogenated ones, as shown in Fig. 4.

The drain current I_d, as a function of input gate bias U_G in the linear region, can be expressed as

$$I_d = K(U_G - U_T)^n U_d \quad (1)$$

where n=1+m and K is

$$K = AC_{ox}W/L, \; K \sim A \quad (2)$$

and C_{ox} is the oxide capacitance. The effective mobility varies with the gate voltage as

$$\mu_{eff} = A(U_G - U_T)^m \quad (3)$$

where *A* is an empirical mobility factor and *m* is a parameter dependent upon the localized states at the grain boundaries.

The calculated effective hole mobilities versus gate voltage for unhydrogenated and hydrogenated TFTs are shown on Fig. 5. The effective hole mobilities for hydrogenated PS TFTs are much higher at corresponding phosphorus concentrations than those of unhydrogenated PS TFTs, while the threshold voltages are lower, as shown in Fig. 5 and Fig. 4, respectively.

The experimental data show that ion implantation of hydrogen in the p-channel polysilicon TFTs improves the device characteristics. The hydrogen in the polysilicon channel passivates the grain boundary states and lowers the grain boundary barriers. As a result, the hole mobilities are increased. The lower threshold voltages of the hydrogenated PS TFTs is understood to be due to passivation of the polyoxide/polysilicon interface states, which is a well known effect.

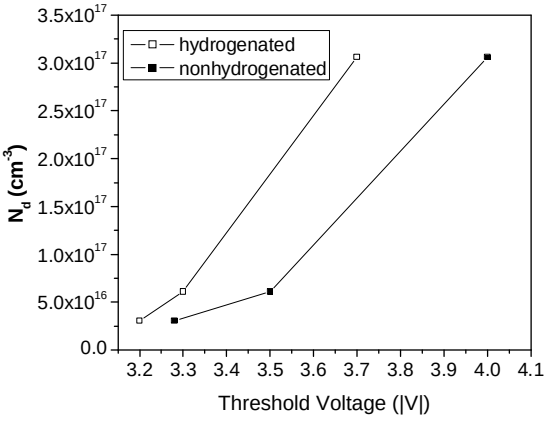

Fig. 4. Threshold voltages of hydrogenated and nonhydrogenated samples at different channel concentrations.

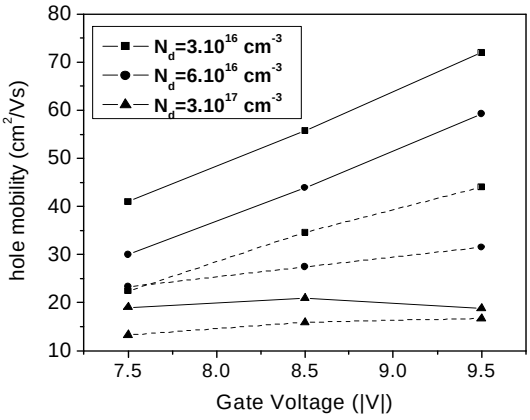

Fig. 5. The changes of hole mobility versus gate voltage. Dash line - unhydrogenated samples, straight line – hydrogenated ones.

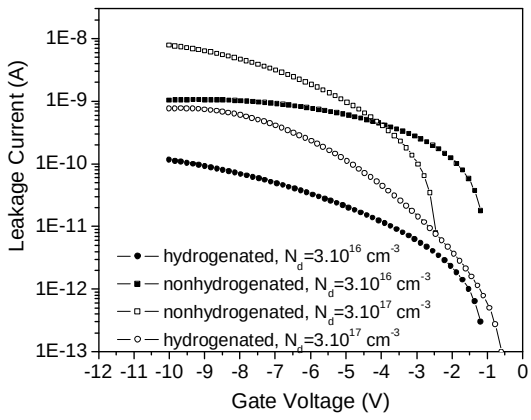

Fig. 6. Leakage currents versus gate voltage for samples with different doping concentrations in the channel.

It was also shown in previous investigations that the lower threshold voltages are due to lower densities of states in the band tails after passivation by ion implantation of hydrogen [3,4]. The results confirm that improvement in the device characteristics is validated for wide range of phosphorus doping concentrations.

Another positive effect of the ion implantaion of PS TFTs is the improvement in the gate oxide leakage currents, as shown in Fig. 6. This effect could be explained by the reduction in the oxide field enhancement due to asperities at the polyoxide/polysilicon interface. The ion implantation introduces neutral electron traps in the oxide, which can capture electrons. These captured charges compensate the oxide field enhancement and lower the leakage currents [2]. The hydrogenation reduces the leakage current by a factor of 10.

4. Conclusions

In order to improve the performance characteristics of PS TFTs, ion implantation of hydrogen must be used. This decreases both the concentration of grain boundary states and the grain boundary potential for phosphorus doped channel polysilicon. Thus, higher carrier mobilities in the inversion layer are obtained. Also, the hydrogen passivates the oxide polysilicon interface states and the fixed oxide charge, resulting in lower threshold voltages. Oxide leakage currents are also reduced. These effects are confirmed for a wide range of phosphorus channel doping and allow more design comfort for the development of PS TFTs circuits. The depth distribution of hydrogen in multilayered structures of PS TFTs can be varied with the ion beam energy. This method could be successfully applied for the correction of transistor characteristics at the wafer level, after the last high temperature processes.

Acknowledgements

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