Journal of Optoelectronics and Advanced Materials Vol. 7, No. 1, February 2005, p. 553 - 556

ELECTRICAL PROPERTIES OF PLASMA-ASSISTED CVD DEPOSITED THIN SILICON OXYNITRIDE FILMS

A. Szekeres[a*], S. Simeonov[a], A. Gushterov[a], T. Nikolova[a], F. Hamelmann[b], U. Heinzmann[b]

[a]Institute of Solid State Physics, Bulgarian Academy of Sciences, 72 Tzarigradsko Chaussee Blvd., 1784 Sofia, Bulgaria
[b]University of Bielefeld, Faculty of Physics, University str. 25, 33615 Bielefeld, Germany

The electrical properties of MIS structures with silicon oxynitride films, deposited at 200 ^{o}C in a RF-plasma CVD reactor using $Si(OC_2H_5)_4$ (TEOS) as a precursor and nitrogen as the gas ambient have been studied. The analysis of the capacitance-voltage and current–voltage characteristics has shown that a larger DC bias yields larger densities of dielectric charge and interface traps in the growing films, and therefore, a lower specific resistivity of the SiO_xN_y films.

(Received December 9, 2004; accepted January 26, 2005)

Keywords: RF plasma CVD deposition, Silicon oxynitride, Oxide charges, Interface traps, Oxide resistivity

1. Introduction

Silicon oxynitride (SiO_xN_y) thin films have found wide areas of application due to important properties, such as a high dielectric constant, resistance to oxidation, low mechanical stress and the possibility of tailoring the film compositions and properties according to industrial needs. In MOS device technology, it is well known that the introduction of a small amount of nitrogen into the SiO_2 gate oxide improves the SiO_2/Si interface properties [1], although the exact role of nitrogen is still not clear. For future miniaturization of MOS devices, SiO_2 has become questionable and SiO_xN_y (or, more accurately, nitrogen doped silicon oxide) is a promising solution [2]. An advantage of its use is that nitrogen is already present at different levels at the interface.

This paper reports the study of the electrical properties of thin silicon oxynitride films deposited by a RF plasma-assisted CVD process through the detailed analysis of capacitance-voltage (C-V) and current –voltage (I-V) characteristics.

2. Experimental details

The plasma-assisted CVD process was performed in a downstream reactor. The plasma source was mounted above the substrate, driven by a 13.54 MHz RF generator with a power of 80 W and nitrogen gas with a flow rate of 4 sccm. The TEOS precursor was introduced into the reactor through a nozzle near the substrate. The total pressure was about 1 Pa during deposition. Double-sided polished wafers of p-type silicon were used as substrates, which were kept at a temperature of 200 °C and biased with a DC voltage of -120 or -600 V.

For the electrical measurements, metal-SiO_xN_y-silicon (MIS) capacitors were formed by the vacuum evaporation of Al dots through a metal mask on the oxide surface and of a continuous Al

* Corresponding author: szekeres@issp.bas.bg

film on the Si rear side. Room temperature high frequency (1 MHz) capacitance-voltage (C-V) and current-voltage (I-V) characteristics were measured, and analysed by the standard high frequency approximation method [3].

3. Results and discussion

Typical C-V characteristics of the MIS structures with silicon oxynitride films are plotted in Fig. 1, in which the arrows show the sweep voltage direction.

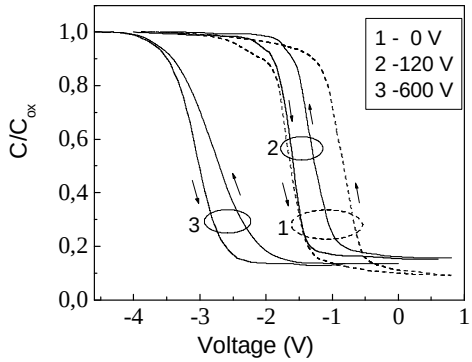

Fig. 1 High frequency (1 MHz) C-V characteristics of a MIS structure with SiO_xN_y films deposited at different DC biases applied to the Si substrate. The arrows show the voltage sweep directions.

As can be seen, the structures are in an unstable state, which is manifested by hysteresis in the C-V curves. By repetition of the sweep cycle, the hysteresis curve moves toward more negative voltages, but its magnitude remains the same. The appearance of such hysteresis indicates that localized spatially distributed interface traps are present further inside the oxide. The stable magnitude of the hysteresis suggests that their distance from the film/substrate interface is approximately the same. The first C-V sweep from the positive to negative voltage direction is shifted less along the voltage axis than all subsequent sweeps, which indicates that these interface traps are donor type. Because the response of the traps depends not only on the voltage but also on the time, it is accepted to identify them as slow interface traps, noted as Q_{slt}. The value of Q_{slt} gradually decreases with increasing DC bias applied to the substrate, as is evident from the decreasing magnitude of the hysteresis. The density of these traps can be estimated from $Q_{slt} = (C_{ox}/q)\Delta V_{hyst}$, where ΔV_{hyst} is the magnitude of the hysteresis in the flatband condition. The Q_{slt} values are given in Table 1.

Table 1. Charge densities (Q_f -fixed oxide charge; Q_{slt} -slow interface traps under flatband conditions; D_{itmg} - averaged interface traps in Si midgap) and the specific resistivity ρ of films deposited at different DC biases applied to the Si substrate.

DC bias (V)	V_{FB} (V)	Q_f (cm^{-2})	Q_{slt} (cm^{-2})	$D_{itmg.}$ ($eV^{-1}cm^{-2}$)	ρ (Ωcm)
0	-0.74	$1.42x10^{11}$	$1.46x10^{11}$	$1.08\ x10^{11}$	$1.83x10^{8}$
-120	-1.28	$2.41x10^{11}$	$6.78x10^{10}$	$1.02x10^{10}$	$2.60x10^{7}$
-600	-2.59	$4.31x10^{11}$	$5.08x10^{10}$	$2.17x10^{11}$	$3.08x10^{6}$

The shift of the flatband voltage from the position for the ideal C-V curve is caused by the generation of oxide defects close to the interface region. These are positively charged, as indicated by the negative shift direction [3]. The density of this co-called fixed oxide charge, Q_f, is estimated from the expression $Q_f = (C_{ox}/q)\Delta V_{FB}$, where ΔV_{FB} is the difference between the experimental and

theoretical flatband voltages. The calculated Q_f values are also given in Table 1. It is observed that although the Q_f density increases with increasing DC bias, it remains considerably low in comparison to that for a standard SiO_2/Si structure before any annealing steps [4,5].

The steep slopes of the C-V curves suggest a rather low concentration of traps localized at the film/substrate interface. A rough estimation of the density of the interface traps, D_{it}, energetically situated between the Fermi level, E_F, and the Si midgap energy level, E_i, can be made from the relation of $D_{itmg} = (C_{ox}/q)(V_{FB}-V_{mg})/(E_F-E_i)$, where, D_{itmg} is the averaged density of these traps and V_{mg} is the voltage at midgap position. The D_{itmg} values, presented in Table 1, are of order of 10^{11} $eV^{-1}cm^{-2}$, being typical for a conventional SiO_2/Si structure only after some annealing steps [4,5]. The MIS structures with a SiO_xN_y film deposited on the Si under a bias of –120 V even show an order of magnitude lower interface trap density (see Table 1).

More precise information about the interface traps D_{it} is obtained from the comparison of the experimental and corresponding ideal C-V curves, as the interface trap density is calculated from the expression $D_{it} = dQ_{it}/dV_s = d[(C_{ox}/q)(V_{exp}-V_i)]/dV_s$, where V_s is the surface potential [3]. The energetic distribution of D_{it} is shown in Fig. 2. The curves are characterized by a wide U-shape with densities well below 10^{12} $eV^{-1}cm^{-2}$ in almost the whole studied region, and with a monotonic increase on approaching the bandgap edges. Around midgap, the D_{it} densities for films grown without or under a small applied bias, are an order of magnitude smaller (below 10^{11} $eV^{-1}cm^{-2}$) than those ($4\text{-}5 \times 10^{11}$ $eV^{-1}cm^{-2}$) for films grown under a bias of 600 V. Apparently, a higher electric field causes a more disordered oxide structure and distorted chemical bonds, these being the precursors of carrier traps. The evidence for this suggestion is the uniformly enhanced and featureless distribution of the interface traps throughout in Si gap (see the 600 V curve in Fig. 2).

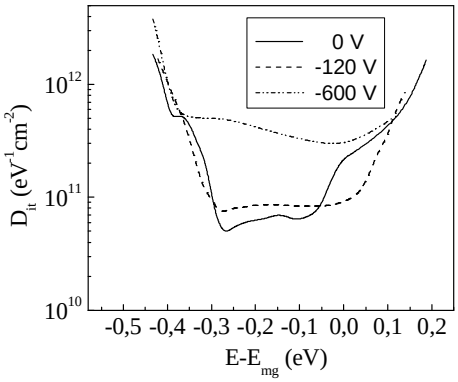

Fig. 2. Energy distribution of the density of interface traps D_{it} in the Si bandgap. The films were deposited at different DC biases applied to the Si substrate, as in the insertion.

The low densities of interface traps, together with the low density of fixed oxide charges, indicate a more perfect interface region. It is known that the SiO_2/Si interface region is structurally imperfect, due to the distorted Si-O_4 tetrahedron network resulting from high stress/strain associated with the volume expansion of SiO_2. However, in SiON, the nitrogen is substitutional for oxygen. The replacement of strained and weak Si-O bonds by strong and rigid Si-N bonds [6] results in the release of structural strains and leads to a reduction of the defect concentration. In addition, N atoms at the interface can be bonded to substrate Si atoms or can replace the weak Si-H bonds. This may remove interface state defects, leading to a significant reduction of the interface trap density. As a result of all these mechanisms, low charge densities are observed.

The conductivity through the SiO_xN_y films can be registered by measuring the I-V characteristics in the accumulation regime. In this case, the capacitance of the MIS structure is maximal and constant, and the applied voltage drops entirely across the deposited film. The forward I-V characteristics of the MIS structures with films deposited under different DC biases applied to the Si substrate are plotted in Fig. 3. As seen, the minimal current density occurs in the case in which no bias is applied to the substrate. Increasing the applied bias leads to a strong enhancement of the current, by several orders of magnitude. Obviously the resistivity of the films deteriorates, indicating the generation of defects inside the dielectric during its growth.

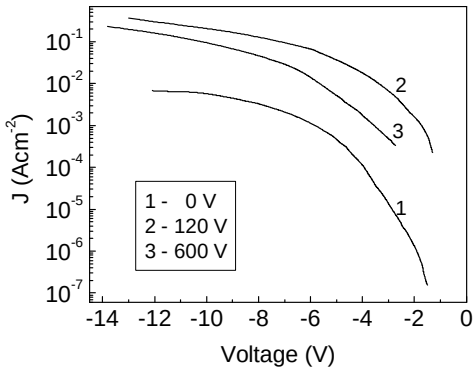

Fig. 3. Current density vs. voltage for films grown with different DC biases applied to the Si substrate.

The specific resistivities, ρ, of the dielectric films were evaluated from the linear parts of the I-V curves, in the voltage range –12 V to –9 V, and the results are given in Table 1.

In comparison to pure SiO_2 films, the specific resistivity of which is of the order of 10^{13} Ωcm [7], silicon oxynitride films have much smaller dielectric resistivities. This indicates that SiO_xN_y films deposited under a given plasma condition possess more defective structures. Our ellipsometric study [8] of these films has shown that a film deposited without applying a bias voltage has the highest nitride volume fraction (17 % Si_3N_4 and 83 % SiO_2), while in the other two kinds of film the nitride fraction drastically decreases at the expense of the oxide fraction. Applying a DC bias to the substrate leads to the introduction of a small amount of unsaturated Si atoms in the oxide, detected as the volume fraction of amorphous Si. In the case of 120 V DC bias, the volume fraction of Si is 0.42 %, while for 600 V it decreases to 0.4 %. The unoxidized and/or unnitridized silicon atoms are electrically active defects in the dielectric network. Hence, they can contribute to the high level of current through the film. Since the concentration of Si atoms in the film decreases with increasing DC bias, a smaller current is observed in the MIS structure with the film deposited at 600 V DC bias (see curve 3 in Fig. 3).

4. Conclusions

From this electrical characterization, we have found that the defect densities in the silicon oxynitride films, deposited by a plasma-assisted CVD process, are comparable to those of a conventional SiO_2 gate dielectric. The low densities of the fixed oxide charge and interface traps, of the order of 10^{11} cm^{-2}, are suggested to be achieved by the replacement of strained Si-O and weak Si-H bonds by strong and rigid Si-N bonds. Applying a DC bias to the Si substrate during film deposition leads to an increase of the leakage current in the oxide. This can be related to the existence of unsaturated Si atoms, a source of defect states.

References

[1] W. L. Hill, E. M. Vogel, V. Misra, P. K. McLarty, J. J. Wortman, IEEE Trans. Electron Devices **43**, 15 (1996).
[2] E. P Gusev, H. C Lu, E. L Garfunkel, T. Gustavson, M. L Green, IBM J. Res. and Development **43**, 265 (1999).
[3] S.M. Sze, Physics of Semiconductor Devices, Chapt.9, Wiley-Interscience, New York 1969.
[4] Y.C. Cheng, Prog. Surf. Sci. **8**, 181 (1977).
[5] S. Alexandrova, A. Szekeres, Phys. Stat. Sol. (a), **92**, 589 (1985).
[6] H.C. Lu, Appl. Phys. Lett. **69**, 2713 (1996).
[7] T.C.R. Skotnicki. Acad. Sci. Paris **1**, (Serie IV) 885 (2000).
[8] A.Szekeres, S. Simeonov, A. Gushterov, T. Nikolova, F. Hamelmann, unpublished.