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HIGH GATE BREAKDOWN VOLTAGE AND LOW LEAKAGE CURRENT USING SELECTIVE CITRIC ETCHANT ON THE SIDEWALL RECESSED AlGaAs/InGaAs PHEMTs

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A novel effective and simple method of selective gate sidewall recess is proposed to expose the low barrier channel at mesa sidewalls during device isolation for $Al_{0.2}Ga_{0.8}As/In_{0.15}Ga_{0.85}As$ PHEMTs (pseudomorphic high electron mobility transistors) by using a newly developed citric-acid-based etchant with high selectivity (>250) for $GaAs/Al_{0.2}Ga_{0.8}As$ or $In_{0.15}Ga_{0.85}As/Al_{0.2}Ga_{0.8}As$ interfaces. After sidewall recess, a revealed cavity will exist between the $In_{0.15}Ga_{0.85}As$ layers and gate metals. Devices with 1×100 μm^2 typically exhibit a very low gate leakage current of 2.4 μA/mm even at V_{GD}=-10V and high gate breakdown voltage over 25V. In our experiments, the maximum gate breakdown voltages for gate-recessed devices with 1×100 μm^2 and 2×100 μm^2 are up to 45V and 38.5V, respectively. As compared to that of non-recessed devices, over three orders of reduction in magnitude of gate leakage currents and over three times of increase in gate breakdown voltages are achieved.

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1. Introduction

Pseudomorphic HEMTs are the state of the art of representative devices for power and low noise applications in microwave and millimeter-wave range. [1-2] However, by the conventional mesa isolation process, the gate may contact the exposed low barrier channel (e.g. GaAs or InGaAs) in AlGaAs/GaAs or AlGaAs/InGaAs HEMTs after gate metallization, leading to an excessive gate leakage current and reduced gate breakdown voltage. The high gate leakage, low breakdown effects will result in power compression, intermodulation distortion and limits its applications. [3]

Some improved methods, for examples, air-bridge, gate passivation and ion implantation have been utilized in HEMT to isolate the sidewall contacts but thay are usually complicated and expensive. [4,5] For selective wet etching, it may be a facile method to eliminate the exposed channel sidewalls between wide-gape layers (e.g. AlGaAs) [6] and is developed to reduce gate leakage current in a decade ago. [7] However, the high selectivity for recessing GaAs or InGaAs over $Al_xGa_{1-x}As$ is ordinarily achieved with high Al mole fraction (x>0.3). [8] A high Al concentration is intolerable since the HEMTs will be sensitive to trapping effects due to DX centers and induce reliability issues. [9] For the long-term stability, the Al mole fraction must be reduced to about 20%, but on the contrary, it will sacrifice the etching selectivity between InGaAs and AlGaAs.

In this work, we propose and demonstrate a simple and effective technique using a newly developed citric acid based etchant to selectively recess the exposed the $In_{0.15}Ga_{0.85}As$ sidewalls of the low barrier channel which is sandwiched between two wide-gap $Al_{0.2}Ga_{0.8}As$ barrier layers. The

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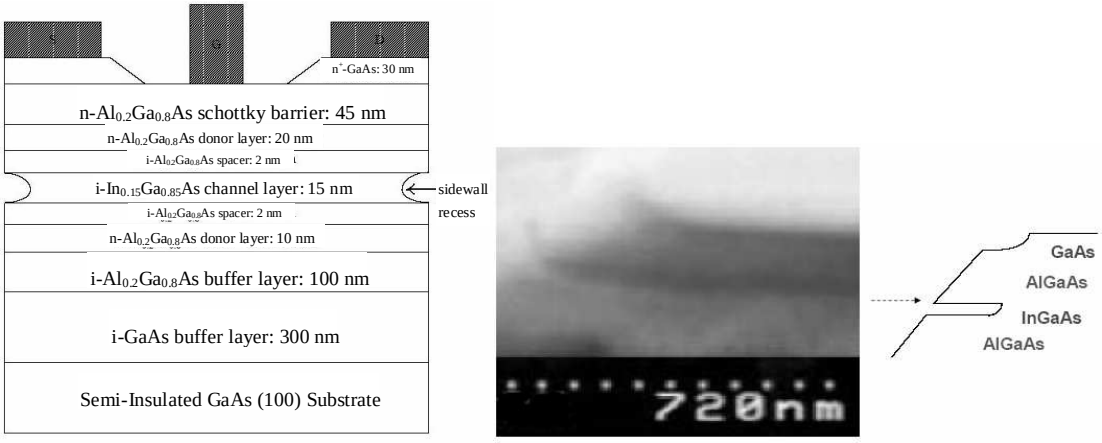
study of recessing the InGaAs channel between the $Al_xGa_{1-x}As$ layers with only 20% Al mole fraction is, to our knowledge, reported for the first time. In addition, devices with 1 μm-gate exhibit good current linearity, in general, low gate leakage of 2.4 μA/mm at V_{GD}=-10 V and high gate to drain breakdown over –25 V, which are superior to those of the PHEMTs without using selective sidewall recess.

2. Device fabrication and experimental process

Epitaxial growth was started on semi-insulated (100) GaAs substrate by molecular beam epitaxy (MBE). The other samples with GaAs/$Al_{0.2}Ga_{0.8}As$ and $In_{0.15}Ga_{0.85}As/Al_{0.2}Ga_{0.8}As$ heterostructures were also grown to investigate the selectivity of the new etching solution. For the PHEMT structure, a 15 nm-thick $In_{0.15}Ga_{0.85}As$ channel was sandwiched between $Al_{0.2}Ga_{0.8}As$ layers and 30 nm-thick n^+ GaAs top layer was grown to form the ohmic contact. The doping concentrations of n-$Al_{0.2}Ga_{0.8}As$ Schottky layers and donor layers are 5×10^{16} cm^{-3} and 1×10^{18} cm^{-3}, respectively. The detailed configuration is shown in Fig. 1(a). During device fabrication, an independent area was defined by mesa isolation, and AuGe/Ni/Au ohmic metals were annealed to the channel at 450 °C for 30 sec. Then, the 1×100 μm^2 gate pattern was defined with Ti/Pt/Au after gate recess. To investigate the effect of the gate sidewalls, the gate pattern was also designed to overlap the mesa sidewalls which were shown in the inset of Fig. 3(a).

The detailed processes of mesa sidewalls are depicted as followings: First, a conventional $1NH_4OH:1H_2O_2:10H_2O$ was used as mesa solution and etched the sample down to the substrate. Then, before removing the photoresist, one set of samples was dipped for 60sec into a newly developed $2CA/63H_2O_2/250H_2O$ etchant at a PH value of 2.4 without additional masks to selectively etch the exposed InGaAs channel in a self-aligned method, i.e., an SEM-measured cavity as shown in Fig. 1(b) is then revealed between two $Al_{0.2}Ga_{0.8}As$ layers. The CA liquid was composed by mixing 1:1 citric acid (monohydrate) with H_2O by weight. The etchant provides a selectivity of 256:1 for GaAs/$Al_{0.2}Ga_{0.8}As$ or $In_{0.15}Ga_{0.85}As/Al_{0.2}Ga_{0.8}As$ configurations (the etching rates of GaAs and $In_xGa_{1-x}As$ for $x<0.2$ are nearly the same in the citric-acid-based solution [10]). The high selectivity is due to the participation of H_2O_2 in the etchant and the optimum volume ratios of CA, H_2O_2 and H_2O [11]. The etching stop mechanism and chemical bonding states were analyzed by X-ray photoelectron spectroscopy (XPS). The experimental I-V characteristics were also measured by HP 4156 semiconductor parameter analyzer.



a b

Fig. 1. (a) Device structure of the studied PHEMT. A cavity is formed between two $Al_{0.2}Ga_{0.8}As$ spacer layers after selective sidewall recess (b) Cross-sectional (011) SEM image and the schematic mesa profile.

3. Results and discussion

Fig. 2 shows the XPS multiplexed core level spectra of Al 2p, Ga 3d and As 3d for the $Al_{0.2}Ga_{0.8}As$ surfaces etched by $CA/H_2O_2/H_2O$ etchant with the solution ratio of (a) 2:33:250

(non-selective etching, i.e., the same etching rate was measured on $Al_{0.2}Ga_{0.8}As$ and GaAs) and (b) 2:63:250 (selective etching), respectively. It is worthy to note that the Al 2p signal contains a peak at 73.6 eV and another peak at 74.9 eV under selective etching condition. It confirms that the shift of Al 2p is corresponding to the formation of Al_2O_3 after using selective etchant. On the other hand, no apparent difference is observed on the Ga and As spectra show the analogous results with those of $Al_{0.2}Ga_{0.8}As$ [11]. The etching stop behavior on $Al_{0.2}Ga_{0.8}As$ can be attributed to the production of insoluble Al_2O_3 on the $Al_{0.2}Ga_{0.8}As$ surface. From experiments, it is found that H_2O_2 (act as oxidizer) content in this work plays an important role to achieve selective etching. The etching rate is much higher in GaAs than in $Al_{0.2}Ga_{0.8}As$ can be attributed to the lack of insoluble Al_2O_3 on the GaAs surface and the Al-O bond is much stronger than the Ga-O and the As-O bonds [12].

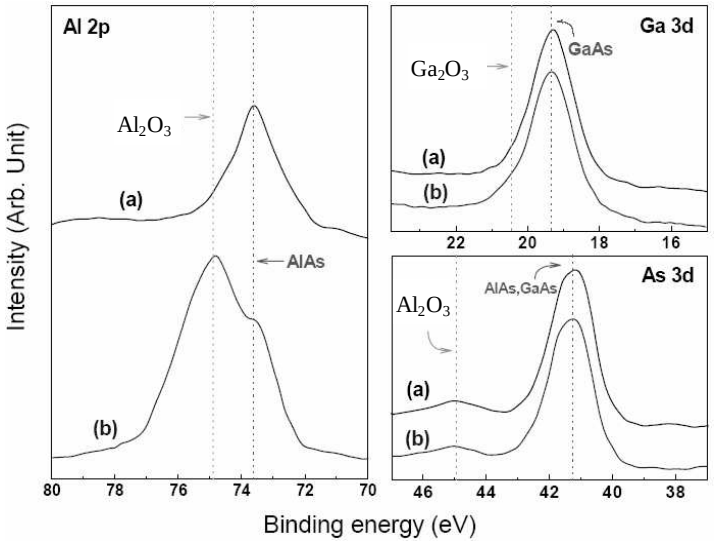
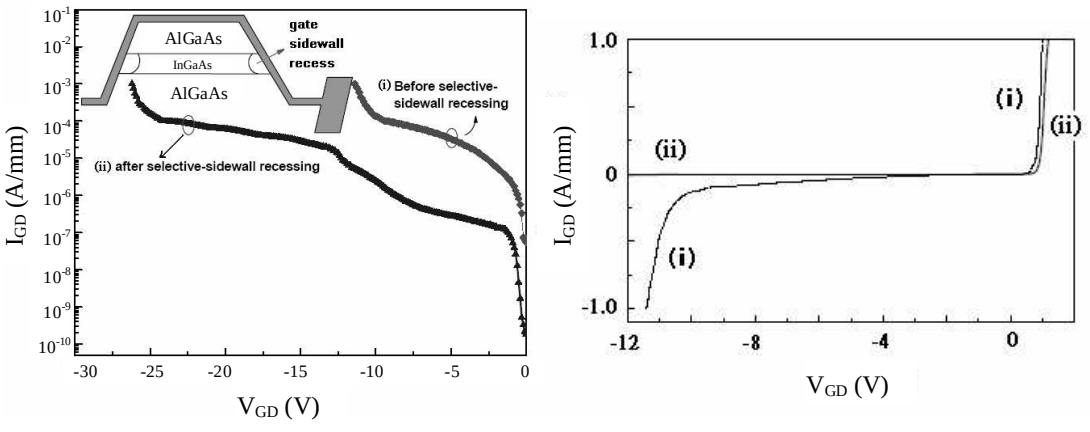


Fig. 2. XPS multiplexed signals for the $Al_{0.2}Ga_{0.8}As$ etched surfaces by $CA/H_2O_2/H_2O$ solution with the ratios of (a) 2:33:250 (b) 2:63:250.

The typical gate-to-drain I-V characteristics of the studied devices with and without selective recess in the channel sidewalls are illustrated as shown in Fig. 3. It is found that the reverse gate breakdown voltage shown in Fig. 3(a) is increased from 10V to 25 V. The forward and reverse gate-to-drain currents in linear scale with and without sidewall recess are also demonstrated in the Fig. 3(b). The gate-to-drain breakdown voltage after sidewall recess is about 25 V at I_G=1 mA/mm, and turn-on voltage is slightly increased from 0.8 V to 0.9 V. For example, the reverse gate leakage current after selective recess is less than 0.3 μA/mm at V_{GD}=-5 V and 2.4 μA/mm at V_{GD}=-10 V. From experiments, it is also found that the gate leakage at V_{GD}=-9 V is 102 μA before sidewall recess, but the best result is 0.06 μA after sidewall recess for devices with 1×100 μm^2. This is significantly reduced over three orders of magnitude in gate leakage.



a b

Fig. 3. Gate to drain I-V characteristics for (i) non-recessed and (ii) gate-recessed devices with (a) log-scale (b) linear-scale.

The gate leakages for non-recessed and gate-recessed devices are summarized in Table 1. These enhanced gate performances are resulted from the elimination of leakage paths from the channel to the gate sidewalls. Fig. 4 shows the best performance on the improvement of gate-recessed devices. For devices with area of 1×100 μm^2 and 2×100 μm^2, the gate breakdown voltages are enhanced from -12.5 V to -45 V and -15.7 V to -38.5 V, respectively. For 1 μm-gate PHEMTs, the improved gate breakdown up to 45 V which is better than that of reported by Lour et al. [13].

Table 1. Summary of typical gate leakages for non-recessed and gate-recessed devices.

Gate Leakage / Gate Length	before sidewall-recess I_{GD}	after sidewall-recess I_{GD}
1 μ m at V_{GD}=-9 V	102 μ A	0.06 μ A
2 μ m at V_{GD}=-13.5 V	85 μ A	0.15 μ A

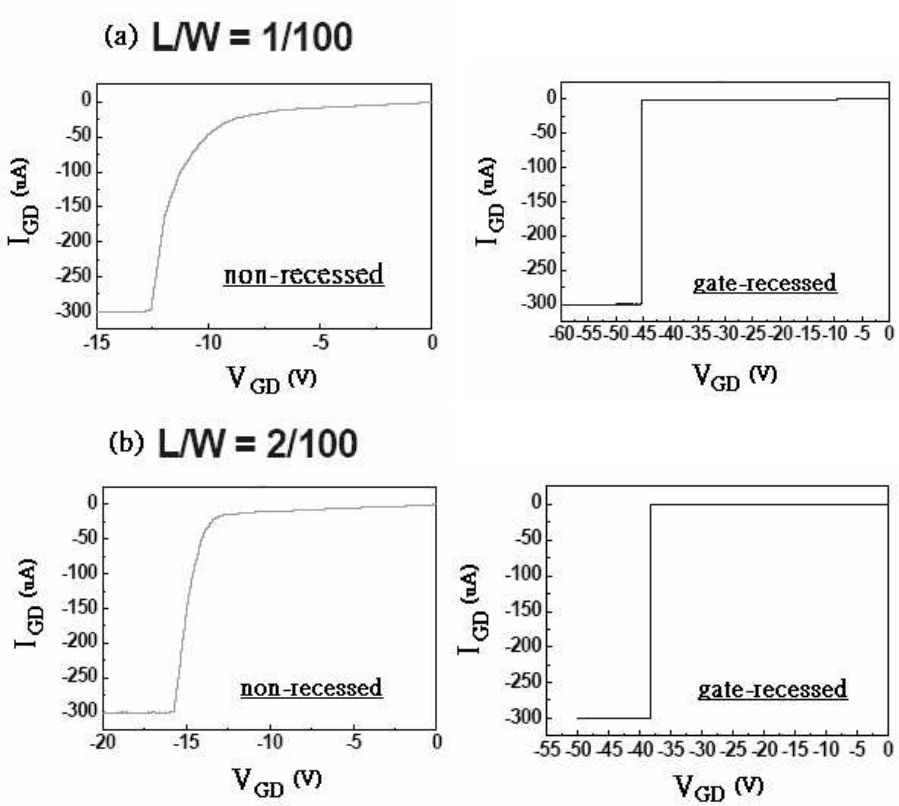


Fig. 4. Measured I_{GD}-V_{GD} Schottky I-V characteristics for devices with 1×100 μm^2 and 2×100 μm^2 under non-recessed and the best gate recessed conditions (85 specimens are measured).

Fig. 5 shows the distribution of gate leakage current in a 3-inch wafer of the studied devices after sidewall recess with an applied gate-to-drain voltage of –12 V. For the 85 specimens, the average of gate leakage current is 7.6 μA/mm at V_{GD}=-12 V, corresponding to the same leakage in non-sidewall recess is V_{GD}=-2.3V. In addition, the measured gate-to-drain breakdown voltage is ranged from –17 V to –45 V with I_{GD}=1mA/mm, which are better than that of non-sidewall recess about 11.5 V. The improved low gate leakage can not only reduce power consumption but also allow operations under RF voltage swings [14].

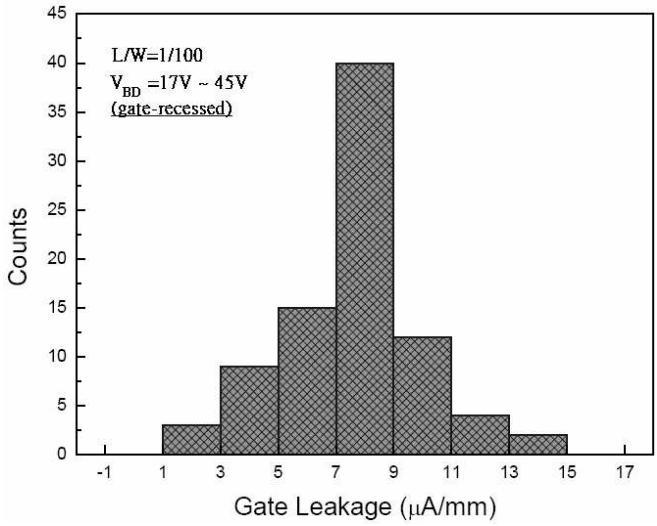


Fig. 5. Histogram of the gate leakage currents at V_{GD}=-12V for the studied devices after sidewall recess. (85 specimens were examined in a 3-inch wafer with the probing system).

The typical common-source characteristics (I_{DS}-V_{DS}) of the proposed devices with and without selective sidewall recess are shown in Fig. 6. The gate is biased from 1 to –2 V with a step voltage of –0.5 V. The studied device shows better pinch-off and saturated characteristics after sidewall recess. The output currents are enhanced under most of the V_{GS} regimes and reduced leakage currents are appeared near the cut-off region. Furthermore, the drain currents could be well controlled up to V_{DS} = 12 V without any kink, hysteresis or breakdown. These remarkable results demonstrate that the sidewall recess actually plays an important role in device performance for the gate control, output current characteristics and breakdown voltage etc.

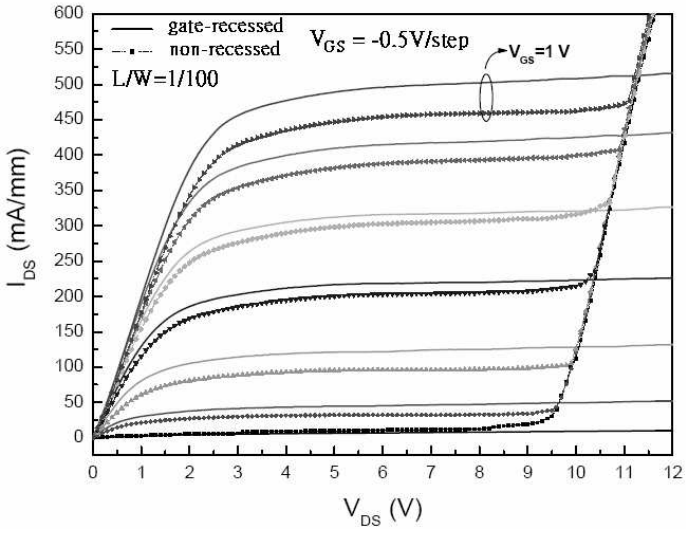


Fig. 6. I_{DS}-V_{DS} characteristics of the 1 × 100 μm^2 device with (solid lines) and without (dashed lines) selective sidewall recess. The gate voltage is from 1V to –2V with –0.5 V/step.

4. Conclusion

A novel selective sidewall recess technique applied to the low barrier channel using a newly developed citric-based etchant has been demonstrated in $In_{0.15}Ga_{0.85}As/Al_{0.2}Ga_{0.8}As$ PHEMTs. The high etching selectivity over 250 for GaAs/ $Al_{0.2}Ga_{0.8}As$ or $In_{0.15}Ga_{0.85}As/Al_{0.2}Ga_{0.8}As$ can be achieved even in a low Al mole fraction of only 20% to avoid the DX centers and reliability issues. This technique with no additional masks can create a cavity to isolate the channel from the gate metals. Sidewall recessed devices with 1×100 μm^2 show distinguished and stable output characteristics, for example, a reduced gate leakage current (<0.3 μA/mm) and high breakdown voltage (>25 V). Not only enhancement over three orders of reduction in magnitude of gate leakage currents has been observed but also greatly improved performance in gate breakdown from 12.5 V up to 45 V has been achieved in this work.

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