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Improving breakdown voltage in AlGaAs/GaAs HEMT by gate oxidation

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A gate-to-drain breakdown voltage of 30 V has been improved to over 62V by liquid phase deposition (LPD) grown native oxides passivated on gate and sidewall positions in AlGaAs/GaAs high electron mobility transistor (HEMT). The transconductance and current density of a 1 x 100 μm^2 device at room temperature (77 K) are 245 (423) mS/mm and 29 (37) mA/mm, respectively. The measured cut-off frequency, f_T, is up to 23 GHz. From experiments, it is found that an enhanced good linearity AlGaAs/GaAs HEMT by native oxides passivation have been successful fabricated and demonstrated in both dc and ac properties.

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1. Introduction

In conventional metal-semiconductor FETs (MESFETs), the electrons are obtained by incorporating donor impurities sharing the same space with electrons and interact with them. Increased electron concentration, necessary for the high currents required for high speed, also means increased donor concentration which leads to more ionized impurity scattering. To improve this kind of FETs, many attentions have been attracted in the performance of high electron mobility transistors (HEMTs) [1-2]. The free electrons of two-dimensional electron gas (2DEG) are allowed to be spatially separated from ionized donors and thereby reducing the influence of impurity scattering on the electron motion. However, the parallel conduction in the doped high-band-gap material may degrade the gate voltage swing. In addition, the output power capability of HEMTs can be limited by gate-to-drain breakdown mechanisms as well as by the forward biased current drawn by the Schottky gate. Therefore, we are interested in studying single power-supply field effect transistors. Because of band-edge offset and lattice match, most of the reported GaAs-based modulation-doped FETs (MODFETs) are concentrated on lattice-matched $Al_xGa_{1-x}As$/GaAs system but it still exists the drawback of DX centers while x is larger than 0.24 [3]. Over the past years, some heterojunction FETs with remarkable high breakdown voltage have been reported [4-5]. Among them, the wide-gap InGaP layer latticed to GaAs layer is of importance due to highly selective etching rate [6].

In this report, an improved performance in AlGaAs/GaAs HEMT has been fabricated except using other materials just by an easy oxidation method, i.e. LPCEO method, to grow native oxides on gate and its sidewall to enhance the gate-to-drain breakdown voltage. From experiment, it is found that the required high breakdown voltage is further improved due to the elimination of gate recess and gate mesa-sidewall leakage current. The native oxides passivation proposed in this work will offer a simple and low-cost alternative way to obtain the high breakdown phenomenon. Experimentally, good dc and ac linearity has been achieved with a very high breakdown voltage over 62 V.

2. Experimental

AlGaAs/GaAs HEMT structures as shown in Fig. 1 were grown by metal organic chemical vapor deposition (MOCVD) on a semi-insulated GaAs substrate. The buffer layer consists of 0.1 μm-thick undoped GaAs, followed by 0.5 μm-thick undoped GaAs. A 4 nm-thick undoped $Al_{0.2}Ga_{0.8}As$ spacer and 40 nm-thick n-$Al_{0.2}Ga_{0.8}As$ with an Si doping density of $5 \times 10^{17} cm^{-3}$ were then grown on the undoped GaAs, followed by a 2 nm-thick n^+-GaAs cap layer with a concentration of 5×10^{18} cm^{-3}. Hall measurements reveal that the electron mobility is 5700 cm^2/Vs and the electron sheet density is $1.8 \times 10^{12} cm^{-2}$ at room temperature. For design consideration, the

depletion-mode devices have an entirely depleted $Al_{0.2}Ga_{0.8}As$ layer, i.e., the remaining doped layer should be just the thickness to be depleted by the gate Schottky barrier. For enhancement-mode devices, the $Al_{0.2}Ga_{0.8}As$ layer the gate metal is made even thinner so that the built-in voltage depletes not only the $Al_{0.2}Ga_{0.8}As$ layer but also the 2DEG. Before fabricating, the sample was first cleaned by acetone, methanol and H_2O_2 for 5 min., respectively. A $3NH_4OH:1H_2O_2:50H_2O$ etching solution was used to expose the mesa region that reached the GaAs buffer layer. Ohmic contacts of Au/Ge/Ni metal were deposited by evaporation, and then patterned by conventional lift-off, followed by rapid thermal annealing at 450 ^oC for 15 sec. After the top n^+-GaAs ohmic layer, the n^+-GaAs/n-$Al_{0.2}Ga_{0.8}As$ layer was etched using the citric-based selective etchant [7]. Then, a gate photoresist is formed and LPCEO growth solution [8] was used to form the gate oxides for device passivation. The oxidation was performed at 60 ^oC with the growth solution at a PH value of 4.5, yielding an oxidation rate of about 40 nm/h. The oxidized AlGaAs around gate recess as shown in Fig. 1 is found to be a composite of Ga_2O_3, As_2O_3 and Al_2O_3. But, on the other hand, the oxidized GaAs around gate mesa sidewall is found to be a composite of Ga_2O_3, As_2O_3. After native oxide growth, the device was baking at 450 ^oC for 10sec to eliminate the H_2O on the device surface. The typical interface trap density in AlGaAs is about $2 \times 10^{12}/cm^2eV$, which is still higher than that of GaAs. Finally, the gate electrode was formed by lift-off with Al metal on the gate recess and the gate sidewall oxide. Fig. 2 schematically depicts the structure of the device passivated with native oxide on the etched sidewall. A single finger device area was 1 μm × 100 μm with a drain-to-source spacing of 5 μm was fabricated for the studied AlGaAs/GaAs HEMT.

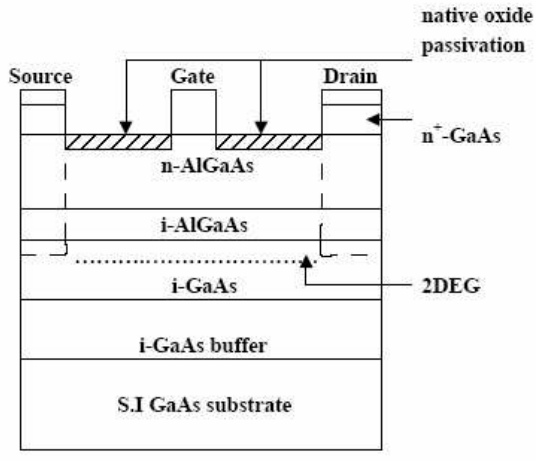

Fig. 1. Cross-sectional structure of the fabricated AlGaAs/GaAs HEMT.

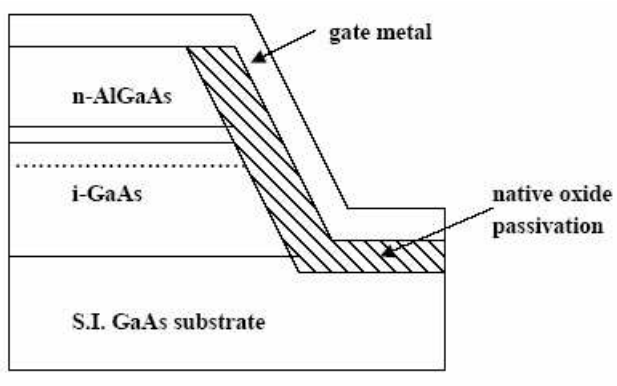

Fig. 2. Cross-sectional view of gate mesa sidewall with native oxide passivation.

3. Results and discussion

Fig. 3 shows the gate-to-drain current-voltage characteristics. It is found that the gate-to-drain breakdown voltage before growing native oxides is 30 V (I_G=18 nA/mm). An undoped AlGaAs layer well acts as a spacer and electrons coming from two 2DEG are confined. The measured breakdown voltage further increases to about 62 V after gate recess and gate sidewall oxide passivation. We obtain a very low leakage current of 10 nA/mm at breakdown voltage –62 V. Clearly, this excellent behavior is primarily attributed to the employment of the selective etching process and native oxides passivation can effectively eliminating the gate recess and mesa sidewall gate leakage. Fig. 3 well demonstrates this improvement in gate leakage current. Room temperature common-source current-voltage (I-V) characteristics of the proposed device are shown in Fig. 4(a). The gate-source voltage V_{GS} is applied by –0.1V/step and the maximum V_{GS} is +0.1 V. The available drain saturation current densities at V_{GS}=0, V_{DS}=4V for no passivated and passivated devices are as high as 40 and 45 mA/mm, respectively. These current drives are attributed to the large product of 2DEG concentration and mobility. Both measured threshold voltages are about –0.5 V and –0.7 V, respectively. However, clear enhancement in both current and transconductance is revealed after passivation. When the oxide passivated device is measured at 77 K as shown in Fig. 4(b), the maximum corresponding saturation current at V_{GS}=0, V_{DS}=4 V is increased to 83 mA/mm due to the enhancement of electron mobility at low temperature.

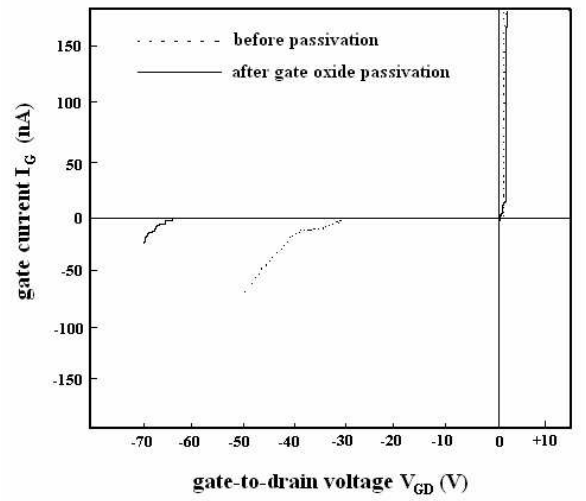

Fig. 3. Measured gate-to-drain current-voltage (I-V) characteristics of the studied device before (dashed line) and after (solid line) oxide passivation.

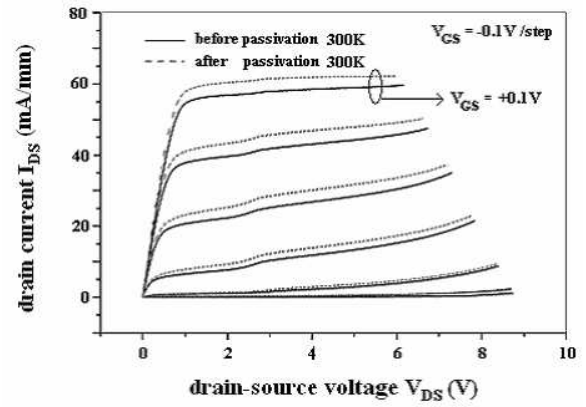

Fig. 4. (a) Measured common-source characteristics of the studied device before (dashed lines) and after (solid lines) oxide passivation at room temperature.

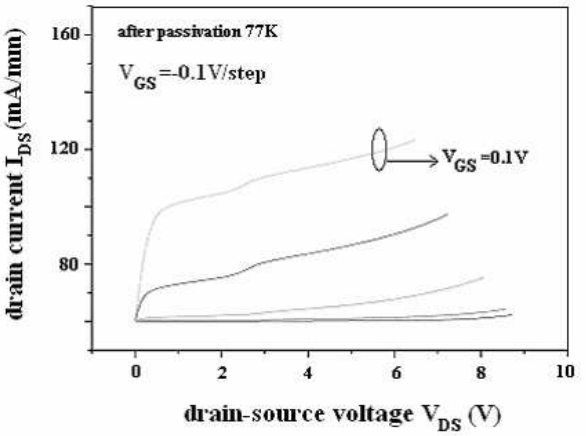

Fig. 4. (b) Measured common-source characteristics of the oxide passivated device at 77 K.

To realize the merits of the proposed structure, the ac frequency responses are shown in Fig. 5. It shows transconductance (g_m) and cut-off frequency (f_T) as a function of drain saturation density. The room temperature and 77 K maximum g_m are 245 and 423 mS/mm, respectively. This good device linearity is mainly attributed to the device oxide passivation. The measured microwave properties of the studied device are investigated by an HP8510B network analyzer in conjunction with cascade probes. The maximum cut-off frequency f_T is about 23 GHz. Good ac linearity is also found in this device. Both dc and ac performances indicate the proposed device is very promising in the microwave applications.

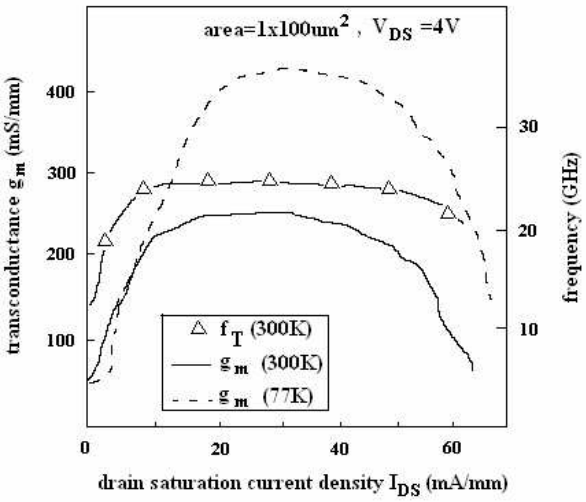

Fig. 5. Measured transconductance g_m at room temperature (77 K) and cut-off frequency (f_T) versus drain saturation current I_{DS}.

4. Conclusions

A new gate oxide passivated AlGaAs/GaAs HEMT with a good linearity both in dc and ac performances has been demonstrated. By growing gate recess and sidewall oxides around the device, we obtain the enhanced breakdown voltage about 62 V with a very low gate leakage current which is twice larger than that of no passivated devices. The improved dc g_m and microwave performance f_T at room temperature are 245 mS/mm and 23 GHz, respectively.

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