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New analytical HFET I – V characteristics model

R. M. ŠAŠIĆ, P. M. LUKIĆ [a*], R. M. RAMOVIĆ [b]
Faculty of Technology and Metallurgy, Karnegijeva 4, Belgrade, Serbia and Montenegro
[a]Faculty of Mechanical Engineering, Kraljice Marije 16, Belgrade, Serbia and Montenegro
[3]Faculty of Electrical Engineering, Bulevar kralja Aleksandra 73, Belgrade, Serbia and Montenegro

In this paper the new analytical model of current – voltage characteristics of a Heterostructure Field Effect Transistor (HFET), is proposed. The model is relatively simple, and at the same time, it describes complex HFET physics. In the new model, most of the parameters have a clear, physical meaning. Presented model includes HFET carrier mobility model, as well as HFET electric field model. Temperature influence is included in the model too. This model is suitable for the design and simulation of different types of HFETs. The results derived from simulations based on the proposed model are in very good agreement with the already known experimental data and theoretically obtained results, available in literature.

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1. Introduction

Heterostructure Field Effect Transistor (HFET) has superior characteristics comparing with standard silicon FET [1 - 11], high operating speed being one of the most important. Like other heterostructure device, HFET consists of very thin layers of different semiconductor materials i. e. donor layer, spacer layer and buffer layer. Doped donor layer, which provides carriers, is made of a semiconductor material with larger band gap, while undoped buffer layer, which collects carriers, is made of a semiconductor material with smaller band gap. Because of asymmetric doping of these joined layers, the quantum well is formed at the buffer side of the heterojunction. Carriers collected in a buffer layer are mostly confined in a quantum well forming a Two-Dimensional Electron Gas (2DEG). Spacer layer is made of the same material as donor layer, but it is undoped [1-8]. Layout of a AlGaAs-GaAs HFET is presented in Fig. 1.

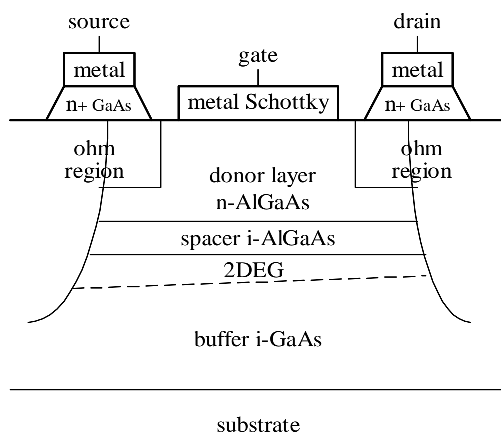

Fig. 1. Layout of a AlGaAs-GaAs HFET.

Speed operation of a HFET is increased because scattering on donor impurities is decreased (due to the spacer layer, which is between donor layer and buffer layer, electrons are additionaly separated from ionized donors). The AlAs-InGaAs-InP lattice-matched HFET, which provides power gain at millimeter frequencies (f_{max}=405GHz), is presently one of the fastest semiconductor transistors [8].

This 2DEG is usually recognized as a HFET's channel. Its charge (actually carriers' surface density) turns out to be controlled by the gate voltage, while lateral transport properties are predominantly governed by drain to source voltage. Following these assumptions, new analytical model of GaAs (or InAs) HFET current – voltage characteristics has been proposed.

2. Proposed model

In spite of numerous attempts performed in the last few years, the drift-diffusion model of carriers' transport in ultra submicron devices has remained the most important one. This is due to the fact that this model strongly relies upon basic concepts of modern transport theory, while at the same time it offers promising capability for construction of models which are simple enough. If Einstein's relation is assumed not to be broken, the infinitesimal drain current turns out to be:

$$dI_D = q_e \cdot W \cdot n(x,y) \cdot dx \cdot \frac{dV}{dy} \cdot \mu(x,y), \qquad (1)$$

where q_e is the electron charge, W is the channel width, n is the 2DEG volume density of the carriers that are confined in the potential well, x is the vertical and y the lateral direction, $V(y)$ denotes quasi-Fermi potential for electrons (being responsible for lateral transport), while μ

is the carriers mobility. Integration over channel, with the respect to its height, implies:

$$I_D = q_e \cdot W \cdot \frac{dV}{dy} \cdot \int_0^{x_{\max}} \mu(x, y) \cdot n(x, y) \cdot dx \qquad (2)$$

Having on mind the proposed dependences $\mu(x, y)$ [1,3] and $n(x, y)$ [1,7], analytical integration of (2) becomes very difficult to be carried out, but for our purpose the approximation of the average mobility is sufficient:

$$I_D = q_e \cdot W \cdot \frac{dV}{dy} \cdot \mu_{eff}(y) \cdot \int_0^{x_{\max}} n(x, y) \cdot dx \qquad (3)$$

or:

$$I_D = q_e \cdot W \cdot \frac{dV}{dy} \cdot \mu_{eff}(y) \cdot n_s(y) \qquad (3a)$$

where n_s is the 2DEG surface density and $\mu_{eff}(y)$ should be evaluated as follows (ψ_s is introduced for the channel's top potential) [1-4]:

$$\mu_{eff}(y) = \frac{\mu_0 \left(\frac{T_r}{T}\right)^{\beta}}{1 + \theta_x \cdot \left.\frac{d\psi_s}{dx}\right|_0} \cdot \frac{1 + \frac{v_s}{\mu_0} \cdot \left(\frac{|E_y|}{E_{0y}}\right)^3}{1 + \left(\frac{|E_y|}{E_{0y}}\right)^4} \qquad (4)$$

In equation (4) μ_0 is the bulk mobility, T_r the room temperature (300 K), T the absolute temperature, β the temperature coefficient with various values used for it between 1.5 and 2, v_s the carriers saturation velocity and E_{0y} the characteristic value of lateral electric field.

Bearing in mind that $\frac{d\psi_s}{dy} = -E_y$ and by using model from [1,2], equation (4) can be rewritten:

$$\mu_{eff}(y) = \frac{\mu_0 \cdot \left(\frac{T_r}{T}\right)^{\beta}}{1 + \theta_x \cdot q_e \cdot \frac{0.85 n_s + n_b}{\varepsilon_b}} \cdot \frac{1 + \frac{v_s}{\mu_0} \cdot \left(\frac{1}{E_{0y}} \cdot \left|\frac{d\psi_s}{dy}\right|\right)^3}{1 + \left(\frac{1}{E_{0y}} \cdot \left|\frac{d\psi_s}{dy}\right|\right)^4} \qquad (5)$$

where n_b is the surface density of ionized acceptors in buffer. Relation (5) is applicable to GaAs, InAs devices as well as for GaN devices if $q_e \cdot \frac{0.85 n_s + n_b}{\varepsilon_b}$ is complemented by a term due to mechanical stress (strained lattices).

While the spatial dependence of quasi-Fermi potential $V(y)$ is not examined in details, the usual next step is to perform the integration of (3a) along the channel:

$$I_D \cdot L = q_e \cdot W \cdot \int_{V_S}^{V_D} \mu_{eff}(y) \cdot n_s(y) \cdot dV \qquad (6)$$

or:

$$I_D = \frac{q_e \cdot W}{L} \cdot \int_{\psi_{sS}}^{\psi_{sD}} \mu_{eff}\left(n_s, \frac{d\psi_s}{dy}\right) \cdot n_s\left(\frac{d\psi_s}{dx}\right) \cdot \frac{dV}{d\psi_s} \cdot d\psi_s \qquad (7)$$

Because of very complex mutual dependences, the equation (7) can hardly be integrated without further approximations. If we expect the linear region and the saturated region to be clearly separated (abrupt transition) in $I_D(V_{DS})$ characteristic, than the first thing to be done is to examine possible mechanisms of saturation appearance. From equation (7) it is obvious that V_{DS} is introduced through the dependence $\psi_{sD}(V_{DS})$, while Fermi-quasipotential is a linear function of V_{DS} ($V(y)$=const.+V_{DS}). Therefore, the first derivate of (7) is investigated:

$$\frac{dI_D}{dV_{DS}} = \frac{q_e \cdot W}{L} \cdot \left[\mu_{eff}\left(n_s, \frac{d\psi_s}{dy}\right) \cdot n_s\left(\frac{d\psi_s}{dx}\right) \cdot \frac{dV}{d\psi_s}\right]_{\psi_{sD}} \cdot \frac{d\psi_{sD}}{dV_{DS}} \qquad (8)$$

In the linear region $\frac{dV}{d\psi_s} \cong 1$ (similar to Si FETs), while μ_{eff} and n_s slowly fall off when V_{DS} rises (ψ_s, $\frac{d\psi_s}{dx}$, $\frac{d\psi_s}{dy}$ rise too and $\frac{d\psi_{sD}}{dV_{DS}}$ also tends to 1). Therefore one can conclude:

In the linear region:

$$\frac{dI_D}{dV_{DS}} > 0 \qquad (9a)$$

$$\frac{d^2 I_D}{dV_{DS}^2} = \frac{q_e \cdot W}{L} \cdot \frac{d}{dV_{DS}}\left[\mu_{eff}\left(n_s, \frac{d\psi_s}{dy}\right) \cdot n_s\left(\frac{d\psi_s}{dx}\right)\right] < 0 \qquad (9b)$$

and the approximate dependence $I_D(V_{DS})$ is verified as:

$$I_D = a \cdot V_{DS} - b \cdot V_{DS}^2 \qquad (10)$$

Although the onset of I_D saturation is usually attributed to velocity saturation, that is not true. The decrease of μ_{eff} and n_s with the increase of electric field strength cannot cause the sharp onset of saturation for some specific V_{DS} value without additional assumptions (equation (8)). According to the solution of Poisson's equation for quasi-one-dimensional case ψ_{SD} can not exceed some specific value (its upper limit) even if V_{DS} further increases, which means:

$$\frac{d\psi_{sD}}{dV_{DS}} = 0 \text{ for short}$$

$$\text{and } \frac{d\psi_{sD}}{dV_{DS}} \geq 0 \text{ for long channel devices} \quad (11)$$

At the same time n_s tends to zero and $\frac{dV}{d\psi_s}$ tends to infinity, but so that the product $n_s \cdot \frac{dV}{d\psi_s}$ remains finite. These conclusions provide that I_D remains nearly unchanged for V_{DS} greater than some specific value:

$$V_{DS}^* \cong \left[(V_{GS} - V_T) - \frac{n_b}{C_G} \right] - \psi_{sS} \quad (12)$$

Coefficients b and I_{DSS} (drain current in saturation) are determined assuming that $I_D(V_{DS})$ characteristic should be continuous and smooth for $V_{DS}=V_{DS}^*$, while parameter a is:

$$a = \left. \frac{dI_D}{dV_{DS}} \right|_{V_{DS}=0} = \frac{q_e \cdot W}{L} \cdot \left[\mu_{eff}\left(n_s, \frac{d\psi_s}{dy} \right) \cdot n_s \left(\frac{d\psi_s}{dx} \right) \right]_{sourceend} \quad (13)$$

If we adopt that $\frac{d\psi_s}{dy}$ can be replaced by its average value $\frac{V_{DS}}{L}$, than the final expressions of our model become:

in linear region:

$$I_D = I_{DSS} \left[2 \cdot \frac{V_{DS}}{V_{DS}^*} - \left(\frac{V_{DS}}{V_{DS}^*} \right)^2 \right] \quad (14)$$

in saturation:

$$I_{DSS} = \frac{1}{2} \cdot \frac{q_e \cdot W}{L} \cdot \frac{\mu_0 \left(\frac{T}{T_r} \right)^\beta \cdot V_{DS}^{*2} \cdot C_G}{1 + \theta_x \cdot \frac{0.85 \cdot C_G \cdot V_{DS}^* + n_b}{\varepsilon_b}} \cdot \frac{1 + \frac{v_s}{\mu_0} \left(\frac{V_{DS}^*}{L \cdot E_{0y}} \right)^3}{1 + \left(\frac{V_{DS}^*}{L \cdot E_{0y}} \right)^4} \quad (15)$$

In spite of the fact that this set of equations (14), (15) seems clumsy, its implementation in more complex circuits simulations is straightforward. All parameters v_s, E_0, β are easily extracted from transport characteristic $v_x(E_y)$ [2]. The only parameter that should be adjusted with the experimentally determined characteristic $I_D(V_{DS})$ remains θ_x (because of numerous effects that affect it, it turns out to be very difficult to calculate it theoretically; for the sake of modelling it is not necessary). Its inverse value can be identified as a critical vertical electric field E_{0x} and is of the order of magnitude 200 kV/cm [1,2].

Presented model belongs to piece-wise ones. Appreciating the fact that continuous models are much more suitable for use in circuit simulators, the best fit to the suggested one should be:

$$I_D(V_{DS}) = I_{DSS} \cdot th\left(\alpha \cdot \frac{V_{DS}}{V_{DS}^*} \right) \quad (16)$$

where α is very close to 2 and I_{DSS} and V_{DS}^* are calculated according to the model proposed in this paper.

3. Results and discussion

Using the proposed model simulations were performed. The following values were used: $\mu(T_r)$ = 9500 cm^2/Vs (GaAs), T_r = 300 K, β = 1.8, v_s = 8.5 × 10^6 cm/s, E_{0x} = 200 kV/cm (adjusted to the experimental values [1,7], E_{0y} = 4k V/cm, $\varepsilon_b = \varepsilon_r\varepsilon_0$ = 13.18 × 8.854187817 × 10^{-12} F/m (GaAs), n_s = 1 × 10^{15} – 2 × 10^{16} m^{-2}, n_b = 1.5 × 10^{14} m^{-2}, W = 20 nm, L = 0.5 μm, C_G = 0.7 × 10^{-3} F/m^2, V_T = 1V.

In Fig. 2 HFET current dependence on drain to source voltage $I_{DS}(V_{DS})$, with gate to source voltage being parameter, is shown. The results are obtained for the temperature T=400 K.

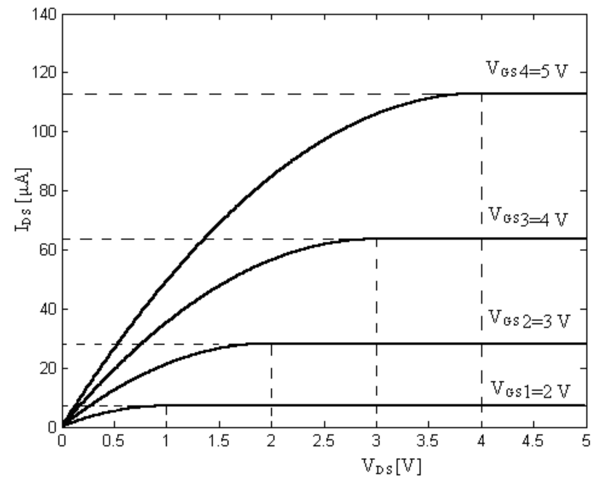

Fig. 2. HFET current I_{DS} versus drain to source voltage V_{DS}, T=400 K.

Linear operating regime and saturation operating regime segments can be easily recognized from the Fig. 2. In linear operating regime, transistor current increases with drain to source voltage as a square function, for fixed gate to source voltage. In saturation regime drain current is constant (the same is usually assumed and proved for the used set of data). HFET reaches saturation for V_{DS} = 1 V if V_{GS} = 2 V (threshold voltage is V_T = 1 V), for V_{DS} = 2 V if V_{GS} = 3 V, for V_{DS} = 3 V if V_{GS} = 4 V etc. Saturation drain current increases for higher gate to source voltages. For

example, $I_{DSS} \approx 30$ μA for $V_{GS} = 3$ V and $I_{DSS} \approx 65$ μA for $V_{GS} = 4$V. All these results are expected.

In Figs. 3 and 4 HFET current dependences on gate to source voltage $I_{DS}(V_{GS})$, with drain to source voltage being parameter, are shown. These results are obtained for temperatures $T = 400$ K (Fig. 3) and T = 600 K (Fig. 4).

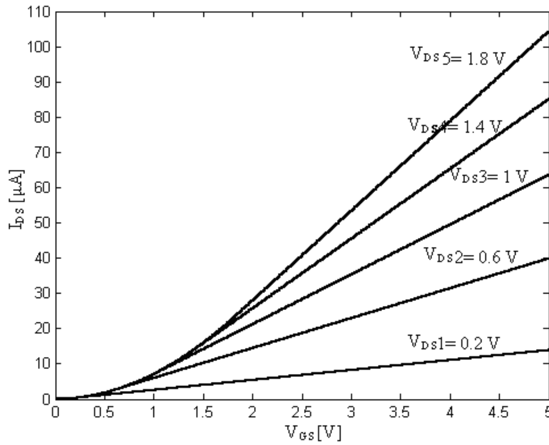

Fig. 3. HFET current I_{DS} versus gate to source voltage V_{GS}, T=400 K.

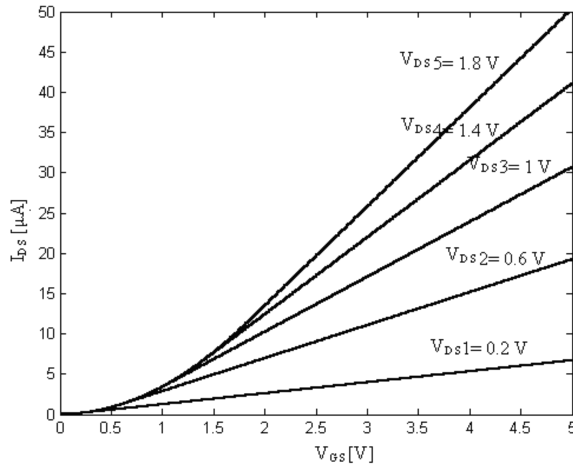

Fig. 4. HFET current I_{DS} versus gate to source voltage V_{GS}, T=600 K.

It can be noticed that current increases when gate to source voltage increases, for fixed drain to source voltage, as expected. Current also increases when drain to source voltage increases. Comparing results presented in Fig. 3 and Fig. 4, it is confirmed that drain current decreases when temperature increases, under other same conditions. For example, $I_{DS} \approx 100$μA for $V_{GS} \approx 4.5$ V and $V_{DS} = 1.8$ V at T = 400 K (Fig. 3) and $I_{DS} \approx 45$ μA for $V_{GS} \approx 4.5$ V and $V_{DS} = 1.8$ V at T = 600 K (Fig. 4).

In Figs. 5 and 6 HFET current dependences on gate to source voltage $I_{DS}(V_{GS})$, with 2DEG surface density concentration being parameter, are shown. The results are obtained for temperatures T=400 K (Fig. 5) and $T = 600$ K (Fig. 6).

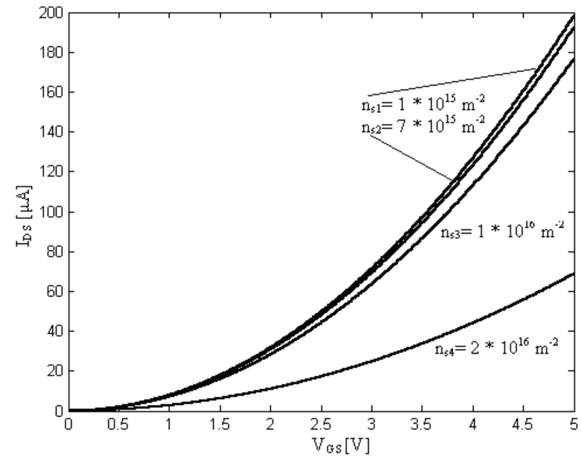

Fig. 5. HFET current I_{DS} versus gate to source voltage V_{GS}, T=400 K.

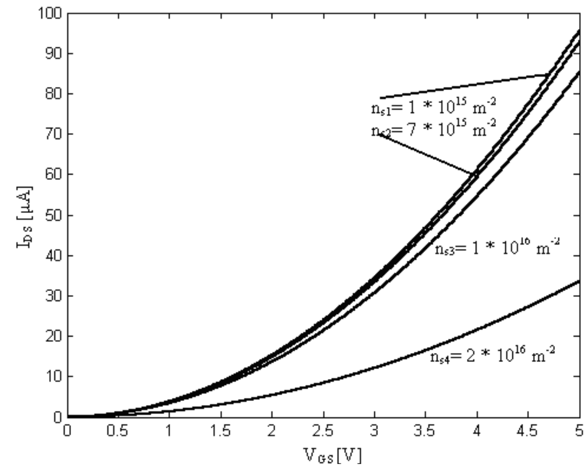

Fig. 6. HFET current I_{DS} versus gate to source voltage V_{GS}, T=600 K.

It can also be noticed that drain current increases with gate to source voltage. Observing results presented in this figures, it is clear that drain current decreases when 2DEG surface density concentration increases. For example, for n_s=2×10^{16} m^{-2} and $V_{GS} = 4.5$ V drain current is $I_{DSS} \approx 38$ μA and for n_s=1×10^{16} m^{-2} and the same $V_{GS} = 4.5$ V drain current is $I_{DS} \approx 160$ μA (Fig. 5). It can be noticed that departures in lower 2DEG surface density concentrations (1×10^{15} m^{-2}- 7×10^{15} m^{-2}) make no significant differences in drain current. One of the reasons is that for lower 2DEG surface density concentration, this value and surface density concentration of ionized acceptors in the buffer become comparable. Comparing results from Fig. 5 and Fig. 6 it can be confirmed that drain current decreases when temperature increases. For example, drain current is $I_{DSS} \approx 160$ μA for n_s = 1×10^{15} m^{-2} and $V_{GS} = 4.5$ V at the temperature $T = 400$ K (Fig. 5) and $I_{DSS} \approx 80$ μA for the same 2DEG surface density concentration n_s = 1×10^{15}m^{-2} and the same gate to source voltage $V_{GS} = 4.5$ V but at the temperature $T = 600$ K (Fig. 6).

4. Conclusions

In this paper a new analytical model of HFET current-voltage characteristics is presented. All basic and significant influences of electrical, technological and environmental parameters on HFET current-voltage characteristics have found its place in the exposed model. Therefore this model can be used for parameters extraction and optimization. Unusual dependence of I-U characteristics on 2DEG surface density concentration is included in the model, too. The model predicts the behavior of the HFET with very good accuracy. Proposed model is applicable to different types of HFETs (except GaN ones; for these ones the polarization field must be accounted for as suggested in the text). Developed model is relatively simple, easily applicable, although it describes very complex physical processes.

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*Corresponding author: plukic@mas.bg.ac.yu