

The experimental estimation of the illumination generation rate in a nano-SOI film

C. RAVARIU^{*}, G. ALECU^a, F. RAVARIU^b

University "Politehnica", Splaiul Independentei, Bucharest, Romania

^aINCIE ICPE-CA, 313 Splaiul Unirii, Bucharest, Romania

^bINCDMT, Bucharest Baneasa, Romania

Some of the most important nowadays SOI technologies, Unibond and SIMOX are in a challenge. The Unibond technique provides thinnest Semiconductor layers (<50 nm) on insulator, while the SIMOX technique has the advantage of a lower cost. The first part of the paper presents these techniques in order to accomplish nano-SOI films. In a second part of the paper, a standard SIMOX wafer, with 200 nm Si-film on 400nm buried oxide on 200 μm Si-substrate was experimentally studied. From the electrical characteristics were deduced the residual net doping concentration in film, the electrical charge from the buried oxide in dark conditions. Then, an average value of the illumination generation rate, in the photoresistance obtained on nano-SOI wafer, was extracted.

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1. Introduction

Usually the SOI acronym means Silicon On Insulator where the Buried OXide (BOX) is the Insulator. This concept must be updated to "Semiconductor On Insulator" for nowadays technologies. The "Semiconductor" could be Silicon [1], Germanium [2], SiC [3], Diamond, [4].

The buried insulator can be oxide, nitride, sapphire [1], quartz, CaF_2 [5] and has a double role in nanostructures: represents a real support for some few atomic layers deposited onto this dielectric and ensures the electrical isolation between the main device and substrate.

In the following paragraph, both SOI nanotechnologies SIMOX and Unibond were described, because the electrical experiments will be related to these structures. The SIMOX process provide n-type film on p-type substrate, while the Unibond or WB process provides the same type of conduction in film and substrate.

2. Two SOI competitors toward nanostructures

Some of the most important nowadays SOI technologies, Unibond and SIMOX are challenging. A brief description of SIMOX technology – Separation by IMplanted Oxygen – comprises the main steps, represented in the Fig. 1a. A deep ion implantation of oxygen, is followed by a short temperature annealing, usually in multistep process. The commonly implantation dose is $1,8 \times 10^{18} \text{O}^+ \text{cm}^{-2}$, at a 190KeV beam energy, [1]. The implantation must be done at a temperature higher than 500 °C, to avoid the amorphization of the substrate. The very high temperature annealing (>1300 °C) allows for the elimination of the defects created during the implantation process and sharp Si/SiO₂ interfaces. A standard process provides: 200 nm silicon on 400 nm buried oxide. The film thicknesses can be adjusted from the energy of implantation.

A schematic description of the Unibond technique, in order to obtain nano-SOI films is shown in Fig. 1b: Gas species (for instance, hydrogen) are first implanted in a substrate A. This step induces the formation of an in-depth weakened layer. Then, the substrate (A) is bonded to a support (B) by wafer bonding technique, [1]. Next, a splitting step, which takes place along the in-depth weakened layer, gives rise to the transfer of a thin layer from the substrate (A) onto the support (B). Finally, a treatment can be performed to remove the rough surface left after splitting. Basic mechanisms involved in splitting of silicon wafers have already extensively been reported. This process allows a large flexibility in layer thickness with very high silicon-thickness homogeneity (better than $\pm 5 \text{ nm}$ over 200-mm wafers), [2].

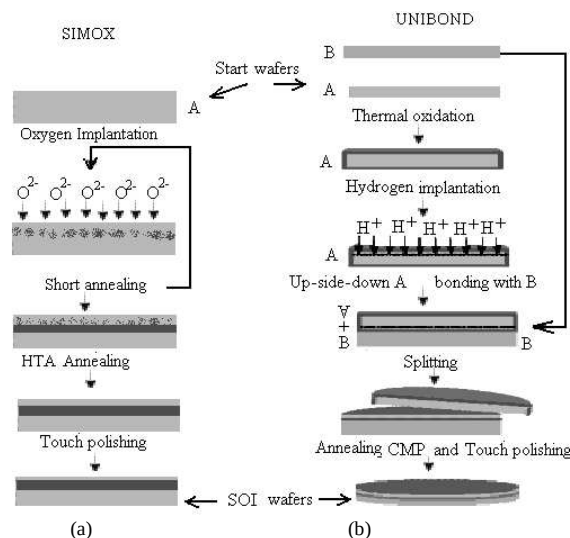


Fig. 1. The schematic SOI process for: (a) SIMOX, (b) Unibond technique.

3. Experiments using pseudo-MOS transistor

The main application of the pseudo-MOS transistor is the electrical characterization of SOI materials with the advantage of a nondestructive technique. After a Separation by Implanted of Oxygen, some ions of Oxygen are captured in the film and acts like donor centers [1]. In this way the film becomes n-type, while the substrate is resting p-type.

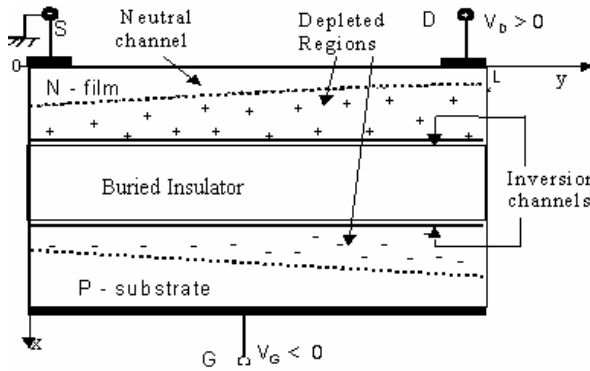


Fig. 2. Biased pseudo-MOS transistor with n-type film and p-type substrate.

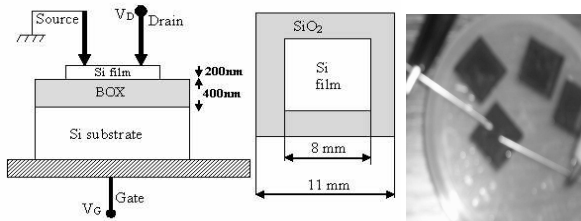
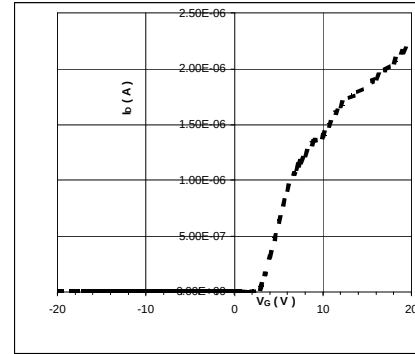
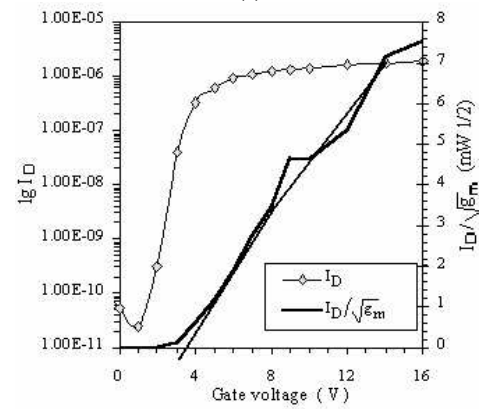


Fig. 3. The top view of the SOI sample.

The structure of the pseudo-MOS transistor is presented in Fig. 2. The gate is represented by the bottom of the SOI wafer and the source and drain consists of two wires placed on the top of the film, Fig. 3. The gate will be negative biased, in order to deplete and eventually to invert the film bottom. In fig. 4.a are presented the experimental characteristics I_D - V_{GS} for $V_{DS}=0.3$ V. The gate voltage was increased up to +20V in strong accumulation and up to -20 V in strong inversion. The measurements were achieved with a picoamperimeter Keithley 236 and handled with Origin 3. The threshold voltage V_T and the flat-band voltage V_{FB} , were extracted from the $I_D / \sqrt{g_m} - V_G$ curves as is described in [1]. The transconductance $g_m = dI_D/dV_G$ was computed with Origin 3 and finally curves are available in Fig. 4b.



(a)



(b)

Fig. 4. (a) The I_D - V_G characteristics at linear scale at $V_{DS}=0.3$ V; (b) the $I_D / \sqrt{g_m}(V_G)$ curves computed at $V_{DS}=0.3$ V.

For fully-depleted pseudo-MOS transistor, the analytical models for the threshold and flat-band voltages was extracted, [3]:

$$V_T = -2\phi_{F1} \left(1 + \frac{\epsilon_{Si}}{\epsilon_{ox}} \frac{x_{ox}}{x_{Si}} \right) - \frac{qN_D}{\epsilon_{ox}} x_{Si} x_{ox} - 2\phi_{F2} \quad (1)$$

$$V_{FB} = -\frac{Q_{ox}}{2C_{ox}} x_{ox} - \frac{Q_{ox}^2}{2q\epsilon_{Si}N_A} + \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} + \phi_{MS} \quad (2)$$

where N_D - doping concentration in n-type film; N_A - doping in p-type substrate, x_{Si}, x_{Si2} - film, respectively substrate thickness; x_{Si} - film thickness; x_{ox} - Buried Insulator thickness; ϵ_{Si} - dielectric permittivity of Silicon, ϵ_{ox} - dielectric permittivity of buried insulator; $C_{Si} = \epsilon_{Si}/x_{Si}$, $C_{ox} = \epsilon_{ox}/x_{ox}$ - specific capacitance of the film, respectively buried insulator; V_G - the gate voltage; $\phi_{F1,2}$ - Fermi potential in film, respectively in substrate, ϕ_{MS} is the metal-semiconductor work-function.

The measured threshold and flat-band voltages, V_T , V_{FB} , were extracted from I_D - V_{GS} curves of a pseudo-MOS transistor by Ghibaudo method, [1]. The cross-point of the linear extrapolation of $I_D / \sqrt{g_m} - V_{GS}$ in strong

inversion/accumulation with the horizontal axis gives $V_T=2.3$ V, $|V_{FBM}|=3.4$ V, respectively. The SOI wafer had 200 nm Si-film with 400 nm buried oxide and 200 μ m p-substrate, manufactured in SIMOX process. The work function $\phi_{MS} = -0.6$ V, is known for the Al-Si-n contact. Accordingly with these sizes and the previous extracted parameters, the residual net doping concentration in film $N_D = 5 \times 10^{15} \text{ cm}^{-3}$ and the global electric charge in the buried oxide, $Q_{ox} = 4 \times 10^{12} \text{ e/cm}^2$ resulted from the analytical models (1) and (2). These values are in agreement with the specific SIMOX technology, [1]. All these values were extracted in dark conditions.

4. The illumination generation rate estimation

For the illumination generation rate determination, usually noted by G_L in semiconductor physics, was possible using measurements I_D - V_{GS} in enlightened conditions, with a 60 W bulb.

Starting from the Ohm's law for low V_{DS} voltage, can be written:

$$I_D = \frac{V_{DS}}{R_{ch}(V_{GS})} = V_{DS} \cdot f_g \cdot \sigma \quad (3)$$

where the channel resistance R_{ch} and consequently the conductivity depends on the gate voltage. In dark conditions, the dependence of the drain current against the drain voltage can be written in a point of graph as:

$$I_{Ddark} = qf_g V_{DS} \cdot (p_0 \mu_p + n_0 \mu_n) \quad (4)$$

The p_0 and n_0 are notations for holes and electrons concentrations in dark conditions. Considering the surface mobility for electrons and holes equal with 1/3 from the bulk mobility at a given net doping concentration, results $\mu_n = 450 \text{ cm}^2/\text{Vs}$ and $\mu_p = 220 \text{ cm}^2/\text{Vs}$. The geometrical factor f_g is the same in dark or light conditions, due to the same shape of contacts. In enlightened conditions, the electrons and holes are additionally generated by the light interaction with the film lattice, increasing the drain current:

$$I_{Dlight} = qf_g V_{DS} \cdot [(p_0 + G_L \tau_p) \mu_p + (n_0 + G_L \tau_n) \mu_n] \quad (5)$$

where the electric charge in exces is $G_L \tau_{n,p}$. From the equations (4) and (5) result the illumination generation rate:

$$G_L = \frac{I_{Dlight} - I_{Ddark}}{I_{Ddark}} \cdot \frac{p_0 \mu_p + n_0 \mu_n}{\tau_p \mu_p + \tau_n \mu_n} \quad (6)$$

By applying the relation (6) in three points I_D - V_{GS} from table 1: $V_{G1}=-4\text{V}$, $V_{G2}=-7\text{V}$, $V_{G3}=-10\text{V}$, respectively results for G_L the values from table 1. The pseudo-MOS transistor was operated in strong inversion in order to

assume n_0 negligible and considering the lifetime of carrier from the inversion channel $\tau_p=10^{-4}$ s. By averaging, results $G_L=10^{20} \text{ cm}^{-3}\text{s}^{-1}$.

This value is obviously higher/lower than that from Si bulk where $G_L=10^{22} \text{ cm}^{-3}\text{s}^{-1}$, because here we worked with minority carriers.

Table 1. The measured drain current against the gate voltage at $V_{DS}=+0.3\text{V}$.

V_G (V)	I_{Ddark} (A)	I_{Dlight} (A)	G_L ($\text{cm}^{-3}\text{s}^{-1}$)
-4	1.93E-09	9.56E-09	2.2e+19
-7	5.54E-09	8.23E-09	1.13e+20
-10	6.29E-09	4.32E-09	2.43e+20

5. Special results in 1nm SOI transistor from Atlas simulations

The device architecture preserved just 2 "undulations" of Silicon onto an oxide support; thinning the Si-channel region, the carrier transport was confined. The source and drain regions are n^+ - type Si ($N_D=10^{17} \text{ cm}^{-3}$) with $y_{n+} = 7$ nm, placed at $x_{vacuum} = 3$ nm distance. A thinner p-type Si layer ($N_A=5 \cdot 10^{15} \text{ cm}^{-3}$) links the source and drain regions. The film thickness was varied: $y_{film} = 200$ nm, 10 nm, 1 nm. In Fig. 2 a family of transfer characteristics I_D - V_{GS} was presented. These curves with a maximum prove the Coulomb blockade initiations for $y_{film} \leq 1$ nm.

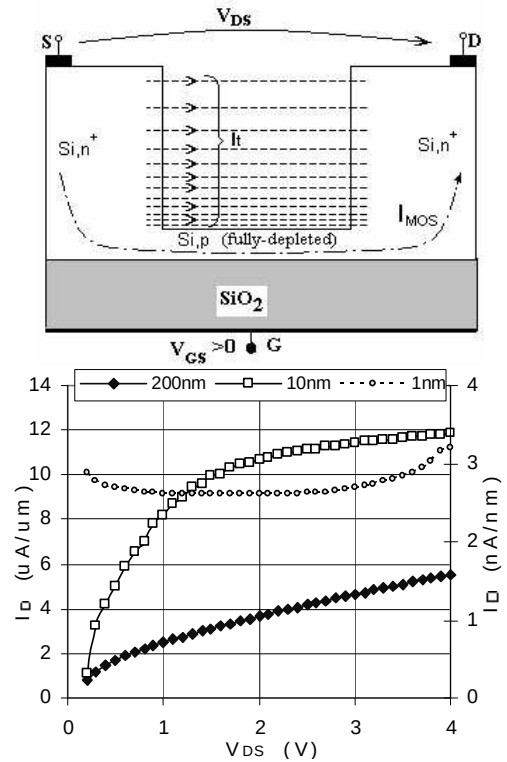


Fig. 2. The simulated I_D - V_{DS} characteristics of a MOS/SOI transistor with different size.

6. Conclusions

One of the most important SOI technologies is SIMOX – Separation by IMplanted OXygen. A standard SIMOX nanostructured wafer with 200 nm Si-film on 400 nm buried oxide on 200 μm Si-substrate was studied in this paper. From experimental transfer characteristics results: $N_D = 5 \times 10^{15} \text{ cm}^{-3} > 10^{15} \text{ cm}^{-3} = N_{\text{substrate}}$ – a validation of the assumption that the residual dopage in SIMOX films overcomes the substrate dopage due to oxygen donors, $Q_{\text{ox}} = 4 \times 10^{12} \text{ e/cm}^2$ – in agreement with the data from literature and the illumination generation rate was estimated at $10^{20} \text{ cm}^{-3} \text{ s}^{-1}$ lower than in Si bulk case as is expected.

Sub 3-nm SOI devices present quantum effects. The Coulomb blockade initiation in the proposed nano-transistor was demonstrated by the simulations: the I_D - V_{GS} curves, where a maximum occurs.

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*Corresponding author: cristir@mcma.pub.ro