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Approaching the limit of the SiO_2 possibilities for application in nanoscale microelectronics

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Silicon dioxide insulating layers play crucial role in the functioning of the contemporary microelectronic devices. The incessant increase of the integration level requires appropriate decreasing of the dimensions of all of the layers. That scaling affects mostly the ultrathin insulating layers with thicknesses approaching now the value of 1 nm, by exposing them to enormous electric fields, reaching the values of order of 10^9 V/m = 1 V/nm. The above high fields produce enormous leakage currents through these insulating layers, owing to different mechanisms, and cause rapid wear-out of the layers leading to their final destruction or loose of the insulating properties. For thicker films the high leakage is a result of the degradation during the fabrication or wear-out during the functioning, while for the extremely thin films (1 nm) fundamental mechanisms like direct tunneling take place. In the present paper our results are presented concerning the improvements of the properties of the insulating films, as well as the possible alternative technologies to obtain insulating films with better quality. The physical mechanisms of thus obtained improvements are explained, in order to benefit at most from technological solutions and find the directions for the further research in the corresponding technologies. Three types of technological solutions are discussed: a) Nitridation of the silicon dioxide layer or growth of an Si-oxynitride layer (SiO_2 and SiO_xN_y layers); b) Growth of a layer of high permittivity (high-*k*) on silicon, specifically Ta_2O_5 (Ta_2O_5/SiO_2 stacked layers) and c) Nitridation of the silicon prior to the Ta_2O_5 deposition, (Ta_2O_5/SiO_xN_y stacked layers). Though the additional technological steps and layers give striking improvements of the dielectric properties, the exceptional properties of the SiO_2 play important role in the conduction mechanisms ensuring the acceptable leakage currents for new generations of integrated microelectronic circuits.

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1. Introduction

The astonishing development of the microelectronic devices during the past half century relied in a great part on the exceptional properties of the silicon dioxide as a functional insulating layer for the metal-oxide-silicon field effect transistors, dynamic random access memories and electrically erasable programmable read only memories. The peculiar structure of the SiO_2 results in extremely low defect densities and leakage currents – the mayor part of the SiO_2 bulk is formed of SiO_4 rigid tetrahedra, connected in an amorphous structure [1], owing to the flexibility of the angle Φ(Si-O-Si), which can vary between 120° and 180° with small changes in energy (14 kJ/mol) and charge. Therefore, the long distance order vanishes not because of the broken bonds but mainly because of the variations of the angle Φ. As a result, a structure with an extremely low density of charges and traps is formed, compared to the majority of the insulators. Nevertheless, the interface with the Si substrate, introduces some imperfections, leading to fixed interfacial charges, Q_{it}, and localized energy states at the interface from the side of the insulator in the forbidden gap of Si, characterized with their interface state densities $D_{it}(E)$, where E is the energy. An interfacial region about 1 nm thick containing suboxides (SiO_2) is present in the SiO_2-Si structures [2,3]. Oxide charges, Q_{ox}, including both the bulk and the interfacial part, as low as 10^{10} cm^{-2} are nowadays obtained with standard technological procedures. Interface state densities at midgap, D_{itm}, as low as 10^{10} $eV^{-1}cm^{-2}$ are obtained simultaneously. In the case of films thicker than approximately 20 nm, at voltages lower than 10 V, extremely low leakage currents are obtained because of the dominant Fowler-Nordheim tunneling mechanism.

The aggressive scaling of the microelectronics devices leads to required oxide thicknesses lower than 4 nm, the limit where the direct tunneling takes place. The future need for oxide thicknesses lower than 1 nm could not be satisfied with the SiO_2 films, because the direct tunneling current would reach unacceptably high values for the leakage. Alternative high dielectric constant (high-*k*) materials are studied in order to obtain the same equivalent thicknesses with physically thicker films, exhibiting much lower leakage currents [4].

Besides the properties of the fresh insulating films, their reliability properties are also important, sometimes much more important. During the high field/current stresses their oxide charges increase, new bulk and interfacial traps are created, the leakage currents increase (stress induced leakage currents, SILC) and various type of breakdown occur. The typical hard destructive dielectric breakdown (HBD) is manifested by a sudden increase of the current at constant voltage or by a sudden decrease of the voltage needed to maintain a given constant value of

the current through the insulating film. In the case of films with lower equivalent thicknesses some other types of breakdown become important, as are the soft breakdown (SBD) and the progressive breakdown (PBD). The SBD event is similar to HBD, but the abrupt parts in the measured stress characteristics are less pronounced and the stress characteristic after the event are slightly modified compared to the part before it. Many SBD events can appear until the final breakdown, or a single HBD can occur after SBD. The so called PBD is detected by the use of other criteria, as is the noise appearance. The different breakdown types were recently reviewed in [5].

In this work we discuss some possible solution for the replacement of the silicon dioxide by other dielectric, especially from the reliability point of view, aiming to indicate the direction for the future development of the technologies able to provide the desired improvements. Technological details on the samples the results for which are presented below are not given here because the main purpose of the work is to discuss the general issues connected with the types of solutions. More details can be found in our works cited below.

2. Rapid thermal oxidation

Several improvements in the insulating film properties can be obtained by use of new fabrication technologies for silicon dioxide.

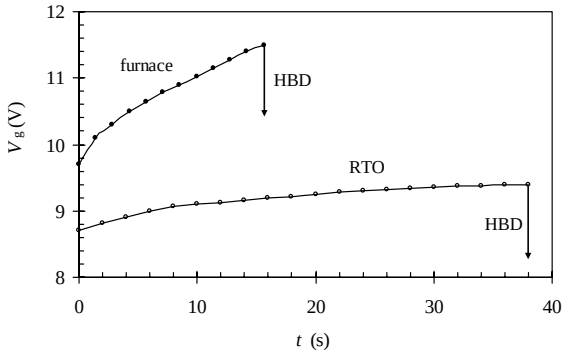

Fig. 1. Comparison between the constant current stress characteristics of a furnace and a rapid thermal oxide grown at 1150 ℃; surface area $S = 3.3 \times 10^{-6}$ cm^{-2}, current density $J = 0.2$ A/cm^2.

It has been shown that the rapid thermal oxides (RTO) have lower oxide charge and interface state densities as well as higher breakdown fields [6,7]. Our results for rapid thermal oxidation at 1150 °C show a visible improvement of the reliability properties of the silicon dioxide films, compared to the "furnace oxides" with gate quality (Fig. 1). As is seen, the increase of the gate voltage (V_g) needed to maintain a given constant value of the injection current through the insulating film with the stress time (t) is much slower for RTO than for the "furnace oxides". This is due to the lower trapping of electrons on the initially existing traps and the traps created during the stress. The arrows show the instant of the breakdown event. Typical hard breakdown events are observed, since the thickness of the insulating film is about 10 nm. Breakdown charges of RTO are significantly higher than these of the furnace grown oxides, for about a factor of two.

The reliability properties of RTO degrade with the further decrease of the thickness. The results obtained for RTO with thicknesses between 6 and 14 nm are shown in Fig. 2. While decreasing the thickness, the breakdown charge (Q_{bd}) for stresses at negative gate decreases. In the case of positive gate Q_{bd} increases attaining significantly higher values than that of the furnace oxides. Nevertheless, for higher stress currents, Q_{bd} at positive gate also decreases with decreasing oxide thickness.

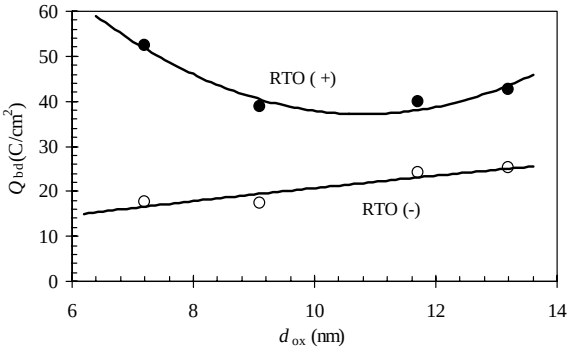

Fig 2. Breakdown charge of the rapid thermally grown oxides (RTO) versus oxide thickness stressed with constant current $J = 0.2$ A/cm^2.

3. Nitridation of the silicon dioxide

Further improvements of the dielectric and reliability properties imposed the use of alternative dielectrics. Between them Si_3N_4 was considered the first as a material already in use in microelectronics. Its dielectric constant (7.5) is higher than that of SiO_2 (3.9). As the deposited Si_3N_4 is of low quality, alternative ways of fabrication were developed. The use of nitrided in ammonia at elevated temperatures SiO_2 insulating layers in integrated circuits was first proposed in [8]. Since the nitridation in ammonia introduces a high amount of hydrogen atoms in the film, oxygen anneal is required in order to exploit the beneficial effects of the nitridation. Thus obtained films are usually named as nitrided reoxidized oxides (ONO). In the beginning it was expected that the mayor improvement of the dielectric and reliability properties can be obtained for heavy nitridations, leading to a composition close to the stoichiometric Si_3N_4. This was assumed on the bases of the higher values of the binding energies in Si_3N_4 than in SiO_2. It was later shown that the optimum improvements can be reached at moderate rapid thermal nitridations, where the composition is that of an oxynitride, SiO_xN_y [9]. Our investigations resulted in an optimum ONO structure from the reliability point of view at relatively light nitridations, where the amount of nitrogen in the films is very low (of order of 1 %). An optimum for nitridations in

ammonia during 4 s at 1100 °C was fount for the films grown, nitrided and oxygen annealed in a rapid thermal reactor (RTONO) [10].

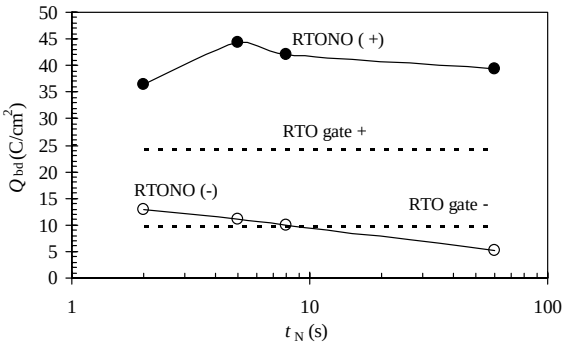

Fig. 3. Breakdown charge of the oxygen annealed nitrided rapid thermally grown oxides (RTONO) versus nitridation time; constant current stress density $J = 3$ A/cm^2.

In Fig. 3 the results for Q_{bd} at a high current density (3 A/cm^2) are shown both for positive and negative gate. The horizontal lines correspond to the reference oxide (RTO). An improvement for nitridations shorter than 8 s is obtained independently on the gate polarity. Longer nitridations are useless or even harmful, particularly in the case of the gate negatively biased. Such a result was explained by the positive effect of the nitrogen incorporation at SiO_2/Si interface, which is the most flimsy part of the structure, making it more resistant to the stress degradation leading to breakdown. Longer nitridations result in an incorporation of nitrogen in the SiO_2 bulk, where it creates an important amount of defects.

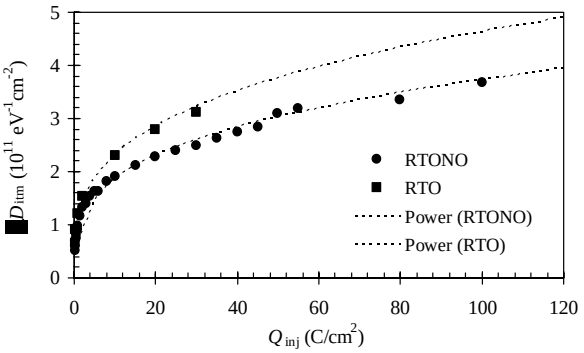

Fig. 4. Increase of the midgap interface state density (D_{itm}) versus injected charge (Q_{inj}) for RTO and RTONO films; constant current stress density $J = 10$ mA/cm^2.

An illustration that the interfaces of the RTONO films are more resistant against the stress than RTO is given in Fig. 4, where the evolution of the midgap interface state densities with the injected charge both for RTO and RTONO are shown. The evolutions follow power laws. More detailed study of the connection between the breakdown and generation of interface states was done in [11].

The oxygen anneal that is unavoidable when nitriding the oxides in ammonia, leads to an excessive oxide growth of about 1 nm. To avoid this problem, growth of the oxynitrides in nitrous oxide was proposed and studied [12]. The growth of the films in nitrous oxide was studied in [13]. As the case of light nitridations presents special interest, we studied the range from 2 to 300 s. It was found that the incorporation of nitrogen atoms at the interface in first few seconds of the film growth creates a barrier against the diffusion of Si atoms from the substrate participating in the further growth of the insulating film. Some $3 \cdot 10^{14}$ cm^{-2} nitrogen atoms when incorporated at the interface can compensate the latice mismatch [14], as obtained while using the idealized cristobalite/silicon(100)-($\sqrt{2} \times \sqrt{2}$) model [15]. During the first phase, the oxynitride film grows to approximately 1.9 nm, then exceptionally slowly, allowing a precise thickness control. Although the value 1.9 nm is noticeably higher than the native oxide thickness (1.4 nm), because of the higher dielectric permittivity, the equivalent oxide thickness can be even lower then 1.4 nm.

4. Tantalum pentoxide films on silicon

Materials with high dielectric permittivity (high-*k*), between them TiO_2, ZrO_2, HfO_2, Al_2O_3, Ta_2O_5 are studied as promising solution for replacing SiO_2. We focus on Ta_2O_5 which was identified to be a solution for dynamic random access memories with equivalent thicknesses between 1 and 5 nm [16–18]. Ta_2O_5 films with excellent electrical and dielectric properties can be obtained by rf sputtering [17]. Oxygen annealing additionally improves their properties [19]. The main disadvantage of the obtained films is the uncontrolled growth of the interfacial layer. The oxxygen annealing besides the positive effects, has the additional growth of the interfacial layer as a negative byproduct. As grown films are Ta_2O_5/SiO_x stacked layers, while the oxygen anneal are stacked Ta_2O_5/SiO_2.

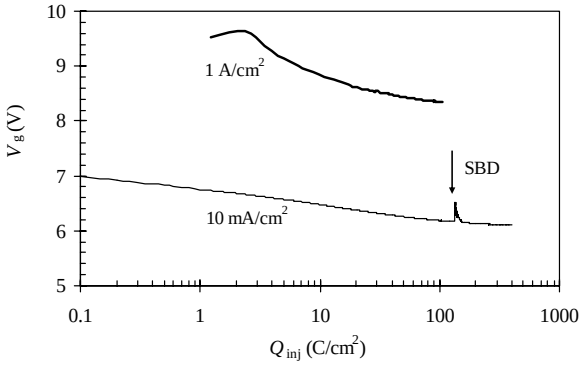

Fig. 5. Constant current stress characteristics of an Al- Ta_2O_5/SiO_2-Si structure.

Constant current stress characteristics of an rf sputtered Ta_2O_5 film (Al-Ta_2O_5/SiO_2-Si structure) for two different current levels are shown in Fig. 5. At higher currents, the gate voltage first increases due to the negative charge trapping, then decreases, as a result of stress induced leakage currents. At lower currents, only the decreasing part is observed. The nature of the stress induced leakage currents was identified to be a result of the effective thinning of the SiO_2 layer of an Al-Ta_2O_5/SiO_2-Si structure by creation of neutral traps during the stress [20]. At higher currents, filling of the neutral traps first dominates, and then the SiO_2 layer thinning becomes dominant. At lower currents only the thinning gives an observable contribution.

The typical stress characteristics do not exhibit hard breakdown. Instead, some kind of soft breakdown, progressive breakdown of a transition between them after 100 C/cm^2 appears (Fig. 5). This breakdown seems to be of a deterministic rather than of a stochastic nature. In a part of the cases HBD at 20–40 C/cm^2 appears. This breakdown is of typically stochastic nature.

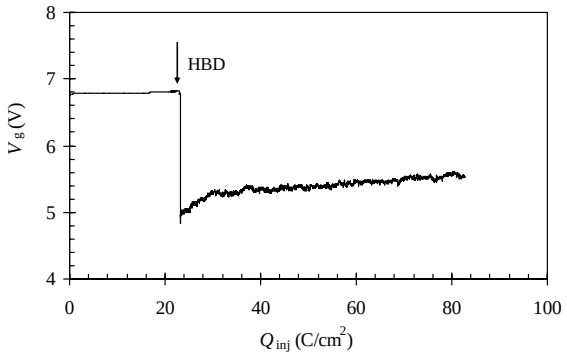

Fig. 6. In a part of the cases HBD occurs: the gate voltage sharply decreases for about 2 V and then noise appears.

The value of the gate voltage after the hard breakdown is relatively high. This is due to the fact that only the SiO_2 layer is broken in this case. More violent stresses also lead to the Ta_2O_5 layer breakdown, in which case the voltage attains values close to zero [5].

5. Leakage current model

Based on the known conduction mechanisms, we proposed a comprehensive model for the I-V characteristics of the metal-Ta_2O_5/SiO_2-Si structures [21]. Hopping conductivity and tunneling in SiO_2 were considered and Poole-Frenkel emission in Ta_2O_5. The current density (J_{PF}) in Ta_2O_5 at a specified field E_{tp} is given with

$$J_{PF} = \sigma_{tp}(0) E_{tp} \exp\left(\frac{1}{kT} \sqrt{\frac{q^3}{\pi \varepsilon_0 K_T}} \sqrt{E_{tp}} \right), \quad (1)$$

where q is the electron charge, $\sigma_{tp}(0)$ is a temperature dependent defect related constant having dimensions of conductivity, k is the Boltzmann constant, ε_0 is the dielectric permittivity in vacuum, K_T is the optical frequency dielectric constant of Ta_2O_5 and E_{tp} is the electric field in Ta_2O_5.

$$J_{so} = \sigma_{so} E_{so} + \frac{q^2}{8\pi h \phi} E_{so}^2 \begin{cases} \exp\left(-\frac{8\pi\sqrt{2m^* q \phi^3}}{3hE_{so}} \left(1 - \left(1 - \frac{d_{so}}{\phi} E_{so} \right)^{\frac{3}{2}} \right) \right) & E_{so} \le \phi / d_{so} \\ \exp\left(-\frac{8\pi\sqrt{2m^* q \phi^3}}{3hE_{so}} \right) & E_{so} \ge \phi / d_{so} \end{cases} \quad (2)$$

where h is the Planck's constant, σ_{so} is the temperature dependent hopping conductivity, m^* is the effective mass of charge carriers in SiO_2, d_{so} is the thickness of the SiO_2 layer, ϕ is the tunneling barrier height, and E_{so} is the field in the SiO_2 layer.

The voltage drop on the oxide (V_{ox}) is

$$V_{ox} = d_{tp} E_{tp} + d_{so} E_{so} , \quad (3)$$

where d_{tp} is the thickness of the Ta_2O_5 layer. While using the standard procedures, the flatband voltage (V_{fb}) and the voltage drop on Si (ϕ_s) were calculated, and V_{ox} for a given V_g determined as

$$V_{ox} = V_g - V_{fb} - \phi_s . \quad (4)$$

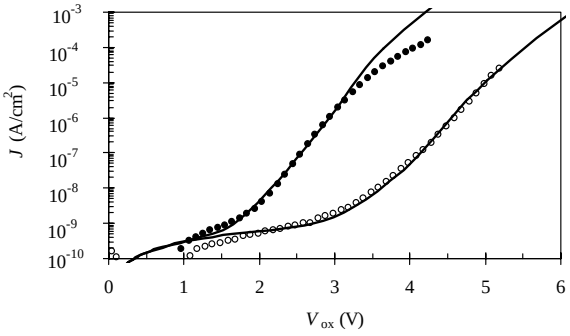

Fig. 7. Theoretical results (solid lines) compared to the experimentally obtained leakage currents versus oxide voltage (open circles – gate, close circuits – positive gate).

The results obtained by the use of this model for an rf sputtered and subsequently oxygen annealed film are shown in Fig. 7. An excellent agreement of the theory with the experiment is obtained. Much lower current for positive gate are explained by the injection of holes from the silicon substrate in this case. Lower values then the theoretical for the positive voltages higher than 3 V are due to the exhaustion of the minority carriers (electrons).

6. Nitridation of the silicon substrate before the Ta_2O_5 growth

Additional interface engineering is required in order to minimize the equivalent thickness in the presence of an interfacial layer. Nitridation of the Si substrate prior to the Ta_2O_5 deposition is a promising tool for further equivalent thickness lowering. Nitridations in NH_3 and N_2O are found to improve the dielectric properties of the Ta_2O_5 films grown on silicon [22]. The interfacial layer thickness can not be made lower than 2.2 nm [22] or 2.65 nm [23], but the equivalent oxide thickness is significantly reduced due to the increased dielectric constant of the interfacial layer. In the case of plasma nitrided substrates in an N_2O ambient, a decrease of about 1 nm of the equivalent thickness was obtained [24]. It has been shown by *ab initio* calculations [25] that for low nitrogen content (less than 25 %) structural pattern of the oxide is preserved in the bulk SiO_xN_y, and the dielectric constant increases mainly because of the variation of the ionic polarizability. As a result, the dielectric constant of the layer increases without significantly degrading the tunneling barriers, thus maintaining the same leakage current while decreasing the equivalent oxide thickness. The above model appears to be useful for the analysis also of these films, both for the initial electrical and dielectric properties and for the reliability properties.

Ta_2O_5 films deposited on plasma nitrided substrates compared to the films grown on bare substrates show higher effective dielectric constant, lower equivalent thickness, lower leakage currents and charge trapping, slower increase of the stress induced leakage currents and higher breakdown charges. Our investigations on the reliability properties of the Ta_2O_5 films grown on silicon are underway and will be published soon.

7. Concluding remarks

Ta_2O_5 films on Si appear as a promising solution for further scaling of dynamic access random memories. While controlling the growth of the interfacial layer (typical phenomenon of most of high-k dielectrics) by appropriate nitridation in NH_3 or N_2O their dielectric properties can be substantially improved. Further studies need to be done in order to identify the optimum technological parameters for obtaining the stacked layers with the lowest equivalent thicknesses that can guarantee acceptably low leakage currents.

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