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Total ionizing dose response of commercial process for synthesis of linear bipolar integrated circuits

V. VUKIĆ*, P. OSMOKROVIĆ[a]
Institute of Electrical Engineering "Nikola Tesla", Koste Glavinića 8a, 11000 Beograd, Serbia
[a]*University of Belgrade, Faculty of Electrical Engineering, Bulevar Kralja Aleksandra 73, p. fah 35 - 54, 11000 Beograd, Serbia*

In this paper are presented results of commercial bipolar integrated circuits examinations in gamma and X radiation fields, for medium dose rate ionizing radiation. Voltage regulators "STMicroelectronics" L4940V5, made by 20V "High Density Super Signal/Power Process" (HDS^2/P^2) were exposed to 1,25 MeV photons of gamma radiation and 150 keV bremsstrahlung photons. By the examination of maximum output current, serial transistor dropout voltage and line regulation characteristics was detected high radiation hardness of the mentioned process. Mechanisms of ionizing radiation influence on semiconductor and insulator are analyzed. The main reasons of high HDS^2/P^2 process radiation reliability were identified.

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1. Introduction

Use of radiation hardened integrated circuits is very important in military, aerospace, nuclear and high-energy physics systems, where the exposure of control and measurement electronic systems to very high doses of radiation is expected. Between 1971. and 2000, more then 4500 incidents were noticed on satelites, airplanes and rockets all over the world [1], assuming that reason for appearance of this incidents is influence of ionizing radiation on electronic components. Today, radiation hardened components are produced by only four manufacturers in the world, having about 100 times higher prices then commercial components with same characteristics [1]. Consequently, use of commercial components in radiation hardened systems becomes of primary interest, also as criteria for definition of radiation hardened commercial processes. Since the need for reliable power supply is especially important in modern digital electronic systems, also as high current density and radiation hardness of bipolar transistors, use of commercial bipolar process for synthesis of voltage regulators designed for operation in radiation environment becomes increasingly important. In the following text will be presented response of one such commercial bipolar process on ionizing radiation.

2. Theory

A. Interaction of ionizing radiation with material

The ionizing radiation damage on bipolar transistor, as the basic element of linear voltage regulators, is manifested primarily in the rupture of the molecule crystal lattice chemical bonds, i.e. charge trap on Si/SiO_2 interfaces or in oxide bulk [2,3]. Trapped charge forms inverse charge region, increasing the generation - recombination currents, causing reduction of minority carriers' lifetime. Macroscopic consequence of this effect is the reduction of common emitter current gain and the appearance of base - emitter contact leakage current [4].

Major influence of ionizing radiation on bipolar transistor common emitter current gain β is realized by the surface recombination mechanism [2]. In contrast to heavy particles (neutrons, protons, ions), whose dominant influence is realized in semiconductor bulk, ionizing radiation photons have dominant effect on semiconductor surface. Physical interpretation of radiation and temperature effects on common emitter current gain can be made by the analysis of Messenger - Spratt relation [2]:

$$\frac{1}{\beta}=\frac{SA_S W}{D_b A_e}+\frac{\sigma_b W}{\sigma_e L_e}+\frac{1}{2}\left(\frac{W}{L_b}\right)^2 \qquad (1)$$

where is: β - common emitter current gain, S - surface recombination velocity, A_S - size of surface recombination area, W - effective base width, D_b - diffusion constant in base, A_e - size of emitter area, σ_b - electrical conductivity in base, σ_e - electrical conductivity in emitter, L_e - diffusion length of minority carriers in emitter, L_b - diffusion length of minority carriers in base. The first term in the equation on the right specifies surface recombination, the second term describes emitter efficiency, while the third term specifies volume recombination in transistor semiconductor. Depending on the type of radiation and temperature conditions, one of specified terms becomes dominant. The second term, $\sigma_b W/\sigma_e L_e$, primarily depends on temperature, so the issue of emitter efficiency is less important on room temperatures, at which tests were performed for the examination of ionizing radiation influence. The third term, $1/2(W/L_b)^2$, which specifies volume recombination, is dominantly influenced by neutron radiation, when the critical parameter for common emitter current gain is minority carrier lifetime in base, τ. Influence of the ionizing radiation on the degradation of common emitter current gain is primary expressed by the first term on the right, SA_sW/D_bA_e, what means that the ionizing radiation realizes its influence on transistor on the surface, opposite to neutron radiation, when dominant effects are exerted in semiconductor bulk. In this case, equation (1) could be simplified by neglecting the second and the third term [2]:

$$\Delta\left(\frac{1}{\beta_S}\right)=\frac{1}{\beta_S}-\frac{1}{\beta_{S0}}\approx\frac{SA_SW}{D_bA_e}=\frac{I_S}{I_e} \qquad (2)$$

where is: β_S - common emitter current gain due to surface recombination, β_{S0} - common emitter current gain due to surface recombination before irradiation ($\beta_S << \beta_{S0}$), I_S - surface recombination current, I_e - emitter current.

After irradiation, the generation of recombination centers begins in transistor base, as well as in oxide layer between base and emitter contacts. Since the electrons mobility is much higher then the holes mobility, holes became trapped, and equivalent positive charge is created in oxide, which tends to recombine with electrons in silicon. For high-quality oxides, with low dielectric loss factor, positive charge trapping process is less expressed, but the recombination process where trapped charges begins to leave the oxide also runs slow [5]. For low-quality oxide insulators, the appearance of leakage current may occur; this current starts to flow through the trapped charge areas in oxide. For outlasting exposures to ionizing radiation, this mechanism may induce breakdown and permanent degradation of integrated circuit. Existence of bias additionally increases the creation of leakage currents, especially in the cases when current flows through the transistors during the irradiation.

Due to lower common emitter current gain and lower operating frequency, PNP transistors are more sensitive to ionizing radiation exposure than NPN transistors [6]. Owing to the surface recombination mechanism, influence of ionizing radiation is more expressed with lateral transistors, having current flow right under the oxide layer, in comparison with vertical transistors, where current flows through the semiconductor bulk [7]. However, technological realization of the lateral transistor is much simpler, and the current gain is also slightly higher than for the vertical transistor.

Type of PNP transistor between the two mentioned is substrate PNP transistor, having the vertical current flow, but substrate is used as the collector region. Radiation hardness of vertical PNP transistor is much higher then hardness of substrate PNP transistor.

The main reason for high radiation hardness of vertical PNP transistor is high implantation of emitter P - type region, also as avoiding of current flow in proximity of oxide surface [6]. Consequently, spreading of N - type base in highly implanted P - type emitter region is weaker expressed in comparison with vertical NPN transistor, having the poorly implanted P - type base, causing the depletion region spreading on the base - emitter junction of vertical NPN transistor. Primary intention of designers concerning the application of ICV PNP technology (Isolated Collector Vertical PNP Transistor) was the decrease of dropout voltage on serial transistor, reduction of collector - emitter leakage current and the improvement of operation stability [8].

The goal of the experiment was the identification of radiation hardness of low dropout voltage regulators with vertical series PNP transistors exposed to two types of ionizing radiation, i.e. influence of γ and X radiation on bipolar integrated circuits design based on vertical bipolar transistors.

B. Characteristics of implemented bipolar process

Synthesis procedure for voltage regulator "STMicroelectronics" L4940V5 is commercial 20V process "Multipower" HDS^2/P^2 ("High Density Super Signal Power Process") [9]. Mentioned process is characterized by the synthesis possibility of MOS and bipolar components on the same wafer, also as synthesis of isolated collector vertical PNP transistor (ICV PNP), vertical NPN transistor (V NPN) and low-leakage diode (LLD) [9]. Procedure of PNP transistor collector isolation was realized by the junction isolation, including additional lateral isolation of base and collector by the local oxide. This process of transistor's areas electrical isolation would significantly reduce integrated circuit's radiation hardness if synthesis process of "nested" emitter was not performed, completely surrounding the emitter area by the highly doped N base region. Applying the "Multipower" HDS^2/P^2 process was obtained the achievement of high series transistor's current densities: J = 6 A/mm^2 (NPN transistor) and J = 2 A/mm^2 (PNP transistor, for V_{sat} = 1V and h_{FE} = 10). Cut-off frequency f_T for small signal transistors in integrated circuit has values in range 0.5 - 1.5 GHz.

As the basic semiconductor material for integrated circuit synthesis was used double layer polycrystalline silicon. At the beginning of the treatment P- silicon crystal was used, with Miller index <100> and specific electrical resistivity ρ = 1-5 Ω·cm. Crystal growing was obtained by the Czochralski's method. In the following text would be presented a short description of technological process for synthesis of the integrated circuit L4940V5.

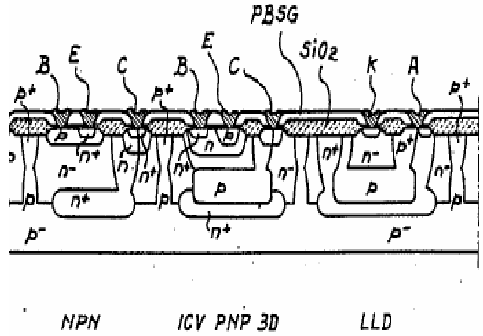

Fig. 1. *Realization of NPN and ICV PNP transistors and low-leakage diode in "Multipower" HDS^2/P^2 process [9].*

After the oxidation of the crystal surface, the first masking operation (total procedure comprises twelve) is performed, followed by the deposition of photoresist. After the wafer illumination through the mask, removal of the unilluminated photoresist is performed. Buried N+ layers are formed by the implantation of antimony ions by the thermal treatment at a temperature of 1200 ^{o}C, lasting about 60 minutes. Afterwards the second masking procedure and implantation of a new layer of photoresist, by the boron ions implantation is performed for creation of P silicon buried layers. Whence the next removal of the photoresist and oxide is finished, epitaxial growth of N- silicon above the P- layer is performed. The specific electrical resistivity of epitaxial layer is ρ = 1-3 Ω·cm, while the thickness of the epitaxial layer is d = 9 - 11 μm. By the oxidation treatment of the wafer surface in a presence of the water vapor at a temperature 920 ^{o}C is realized generation of the silicon oxide insulator layer, thick about 150 nm [9].

During the third masking operation is exerted forming of the collector region P - "wells" of ICV PNP transistors by the implantation of the boron ions of energy 80 keV, until the reaching of the impurities concentration Q = 10^{13} cm^{-2}. Removal of photoresist and the wafer thermal treatment are followed by the silicon nitride (Si_3N_4) deposition from vapor phase on the semiconductor surface, 300 nm thick. The next step is a new masking operation, afterwards are performed successive diffusions, according to the position of photoresist. Areas of Si_3N_4 protected by the photoresist have to be removed by the "plasma attack" [9].

The fifth masking operation precedes the removal of the silicon oxide (SiO_2) layer, afterwards followed by the implantation of the phosphorus ions of energy 80 keV, generating the N+ "sinker". Phosphorus implantation lasts until the achievement of impurities concentration Q = 10^{15} cm^{-2}, afterwards followed by the boron implantation (E = 40 keV), creating the P+ region, with concentration of impurities Q = 10^{15} cm^{-2}. After the removal of photoresist the thick layer of local oxide is formed above the areas uncovered by the Si_3N_4. Silicon oxide layer, about 1 μm thick, is generated by the heating of wafer to a temperature 1000 ^{o}C in a presence of water vapor. After the oxidation treatment is performed removal of Si_3N_4 by the chemical attack, resulting in formation of the SiO_2 layer 70 nm thick at a temperature 875 ^{o}C. By this treatment is realized the connection between the P+ and P junction isolation, i. e. creation of "wall" for isolation of components.

The next steps in a technological treatment are deposition of polycrystalline silicon from the vapor phase, 450 nm thick, silicon doping by phosphorus, masking and removal of polycrystalline silicon from the unmasked regions. By the oxidation of the polycrystalline silicon at a temperature 1100 ^{o}C, during the twenty minutes in the oxidizing atmosphere, the first layer of polycrystalline silicon, necessary for generation of passive components, is obtained. Capacitors are created by the two layers of polycrystalline silicon and the oxide layer. The first layer is heavier doped by the phosphorus, owing to the assurance of a lower surface resistivity [9].

By the seventh masking procedure are defined NPN transistor collector region and ICV PNP transistor base region. Oxide etching is performed until exposing the silicon in this areas, afterwards followed by the phosphorus ion implantation at 100 keV during the achievement of impurities concentration Q = 10^{13} cm^{-2}. Afterwards the resist removal and silicon surface re-oxidation in regions implanted by phosphorus, the new masking is performed by the boron implantation at E = 80 keV, Q = 5×10^{13} cm^{-2} and a thermal treatment implementation for creation of NPN transistor base region, also as ICV PNP transistor collector and emitter region. The next step is creation of NPN transistor's emitter shallow N+ regions and ICV PNP transistor base regions. Oxide removal is performed by the "plasma attack", followed by the arsenic implantation (E = 50 keV, Q = 5×10^{15} cm^{-2}).

Above the complete area of created wafer deposition of insulator SiO_2 layer, 500 nm thick, is done, and above the first layer is deposited the second SiO_2 layer of the same thickness, implanted by phosphorus and boron (PBSG - Phosphorus Boron Silicon Glass). Above the PBSG layer is deposited the alloy with ingredients 99% aluminium - 1% silicon. At the end of integrated circuit's synthesis process removal of the metal from unmasked areas is performed, final isolation layer (SiO_2) deposition implanted by phosphorus and creation of metal contacts with electrodes [9].

3. Experiment

Integrated 5-volt positive voltage regulators "ST Microelectronics" L4940V5 were tested in Institute of Nuclear Sciences "Vinča", in Metrology - Dosimetrical Laboratory. Twenty integrated circuits were separated in four groups. Five unbiased IC's were tested on sources of γ and X radiation each. Next two groups of five voltage regulators were tested with bias and load during the irradiation. In this case input voltage was 7V, while output current was kept on 100 mA. All IC's were exposed to the radiation on the same positions in the vicinity of the sources [10].

A. The Sources of Ionizing Radiation

^{60}Co was used as a source of γ radiation and it was situated in the device for the realization of γ-field, IRPIK-B. The source ^{60}Co activity was, on production date (August 28, 1990.), A=124.1 TBq, and half-life of corresponding radiation source is $T_{1/2}$ = 5.272 years. Accepted mean energy of γ-photons is E_γ = 1.25 MeV. Samples were irradiated in the mouth of collimator.

For the purpose of obtaining X radiation, that is, 150 keV energy photons, dosimetrical generator PHILIPS MG 320 was used. Voltage and current of the roentgen tube MC 321 were set to 300 kV, 10 mA during the experiment. The filtration was performed with aluminum foil, 0.47 mm thick.

Exposition doses measurement was exerted with the cavity ionizing chamber Dosimentor PTW M23361, volume 3×10^{-5} m^3, with uncertainty of measurement ± 2%. With cavity ionizing chamber, reader DI4 was used [10].

B. Electrical testing

Samples of voltage regulators L4940V5 were irradiated in groups of two circuits. Devices were supplied by 10 meter long cables, with total resistance 0,4 Ω. To keep the operation stability, on the ends of cables, i.e. on IC's input contacts, 33 μF electrolytic capacitors were mounted. Beside the supply cables were laid sense cables of the same length. In this manner was enabled direct measurement of IC's voltages and currents during the irradiation. Aluminum heat sinks of thermal resistance 14 K/W were mounted on cases of integrated circuits (plastic, TO-220). Supplies of voltage regulators were realized with a source of DC voltage by which was achieved simultaneous supply of four electrically isolated IC's. Filter and output capacitors were connected according to the IC's manufacturers recommendations, for the purpose of attaining stable operating conditions and suppressing AC voltage component. Current and voltage measurement was carried out with laboratory instruments FLUKE 8050A, whose uncertainty in measurement is 0,03%. All measurements and the irradiation of components were performed on room temperature of 19 ^{o}C. Measured effective value of noise in measuring path was about 200 μV [10].

C. Procedure

Macroscopic values used for the detection of voltage regulator's degradation due to exposure to ionizing radiation are maximum load current, voltage drop on serial transistor and change of output voltage. Examination of maximum output current change was performed in the following way: for constant input voltage equal to 8 V, load current was increased until output voltage dropped to 4.7 V. Lower output voltages are unacceptable for voltage regulator, since the device is beginning to shutdown [11]. Reaching the output voltage equal to 4.7V, a slight increase of load current evokes drop of output voltage to 0V, i.e. device loses regulation ability.

Examination of dropout voltage change on serial transistor was performed in the following way: input voltage was increased until output voltage dropped to 4.9V, for constant output current of 100 mA and 400 mA. Difference between input and output voltage represents dropout voltage on serial transistor for corresponding current. Owing to the decrease of transistor common emitter current gain after exposure to ionizing radiation, output voltage value used to fall below 4.9V; therefore, in order to acquire complete data regarding device functioning ability after irradiation, it is also necessary to obtain information about the change of maximum output voltage as a function of total ionizing doze (TID).

During the line regulation characteristics examinations, values of output voltage are measured for constant output current (0A, 100 mA, 300 mA, 500 mA and 700 mA), while the input voltage is varied (6.5 V, 8 V, 10 V, 12 V and 15 V). Obtained diagrams represent the difference between output voltage of unirradiated circuits and output voltage of components exposed to total ionizing dose (TID) 300 krad(Si). Line regulation tests are the most reliable way for examination of voltage regulators characteristics in a full operating range.

The devices had been irradiated until predetermined total doses were reached, when irradiation was cancelled and all four groups of devices were tested. For the purpose of avoiding the effects of recombination in semiconductor after irradiation, all measurements were performed within the time interval between half an hour and two hours after the exposure, in order to avoid device annealing, i.e. recombination of trapped charge. After electrical tests for certain absorbed dose level were done, irradiation of IC's was continued. Devices in γ radiation field were exposed to total dose of 300 krad(Si), with dose rate of 5.5 rad(Si)/s, while the samples in X radiation field absorbed dose of 100 krad(Si), with dose rate of 11.6 rad(Si)/s. Devices in γ radiation field absorbed dose 50 krad(Si) during the day, while the samples have been irradiated during the night until they absorbed TID 300 krad(Si). Also in this case, all examinations had been performed for less then two hours after irradiation.

4. Results

A. Maximum Output Current

In Fig. 1 is shown mean value of maximum output current of IC's L4940V5 after exposure of unbiased and biased samples to γ radiation, while the change of maximum output current after exposure of samples to X radiation is shown in Fig. 2. Data shown in the figures were obtained by testing "STMicroelectronics" devices, batch GKOXO VW CHN 423, made in China.

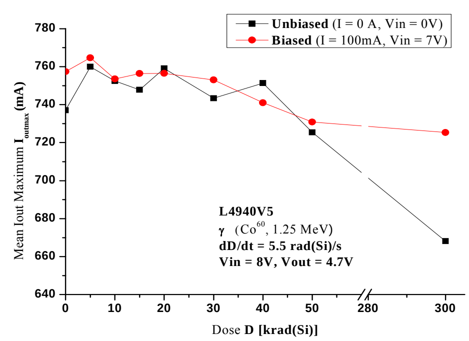

Fig. 1. Change of maximum output current on serial transistor of voltage regulator L4940V5 under influence of γ radiation.

Differences in initial values of maximum current, for TID 0 rad, result from the variety of values of this parameter for tested samples in the batch, used for calculation of mean value. Devices were exposed to γ radiation ionizing dose of 300 krad(Si). Devices were exposed to the influence of X radiation until they absorbed TID 100 krad(Si).

Presented results lead to conclusion that IC L4940V5, i.e. technology process ICV PNP HDS^2 P^2 (Isolated Collector Vertical PNP Transistor - High Density Super Signal / Power Process), shown radiation hardness to the influence of γ radiation dose 300 krad(Si), for medium dose rate of 1.25 MeV photons. Examination results show that unbiased device L4940V5 is more sensitive to the influence of high TID than biased device; these results also show that after unbiased circuits had absorbed γ radiation dose 300 krad(Si) their functioning degradation didn't occur. Exposure of unbiased devices to the dose of 300 krad(Si) leads to the decrease of maximum output current for approximately 10%. Effect of trapped charge recombination, i.e. circuit annealing, is more expressed for biased devices, as can be seen in Fig. 1. For radiation doses of less then 100 krad(Si) significant differences between biased and unbiased devices are not reported. The reason for slightly better results of biased circuits, in comparison with unbiased, lay in absence of shallow charge traps, which tend to recombine with electrons during the current flow below the oxide layer. Very high ionizing dose level absorbed before the manifestation of positive trapped charge existence in the oxide layer indicates high quality of isolation oxide, i. e. low oxide dielectric loss factor.

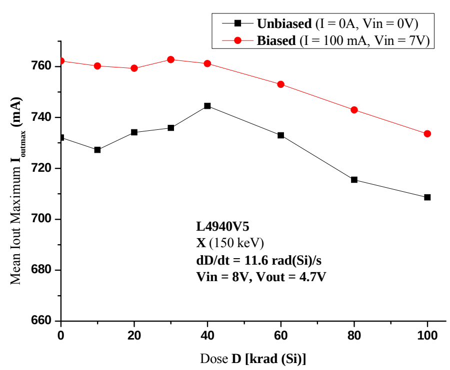

Fig. 2. Change of maximum output current on serial transistor of voltage regulator L4940V5 under influence of X radiation.

B. Dropout Voltage on Serial PNP transistor

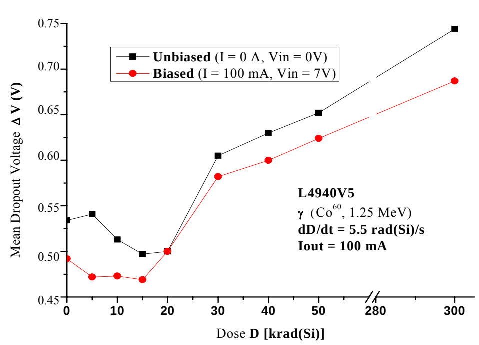

Fig. 3. Change of mean dropout voltage on serial transistor of voltage regulator L4940V5 under influence of γ radiation.

Fig. 3 shows the change of the mean dropout voltage on serial transistor of circuit L4940V5, as a function of γ radiation TID. It can be seen that there exists a trend of slow increase of dropout voltage on serial transistor, which is more significant for unbiased devices. Operation correctness can be seen even after exposure to very high ionizing doses. Shown variations of serial transistor dropout voltage are acceptable, and they do not have drastic influence on device characteristics deterioration. Not one of the five devices, neither in unbiased test conditions, nor under the presence of load and input voltage during irradiation, ceased functioning; the output voltage also did not fall below the boundary of 4.9 V.

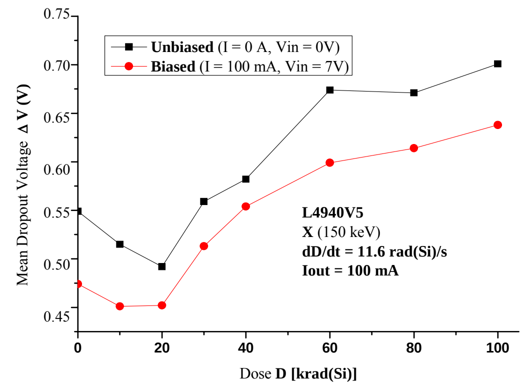

Fig. 4. Change of mean dropout voltage on serial transistor of voltage regulator L4940V5 under influence of Xγ radiation.

Fig. 4 shows a change of mean serial transistor dropout voltage as a function of X radiation TID. Also, during the exposure of devices to the influence of lower energy photons, there exists the same trend of mean dropout voltage increase, as in the case of irradiation in ^{60}Co field. Similarly to the previous case, unbiased IC's show slightly higher sensitivity to the influence of ionizing radiation.

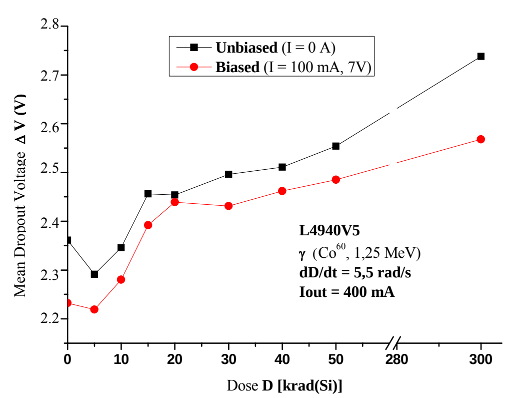

Fig. 5. Change of mean dropout voltage on serial transistor of voltage regulator L4940V5 under influence of γ radiation.

In Fig. 5 is shown change of mean serial transistor dropout voltage as a function of total ionizing dose of γ radiation, during the examination with bias current equal to 400 mA. In Fig. 6 is shown the same function after components' irradiation in the X radiation field. Stability of device's dropout voltage and IC's functionality after absorption of high total doses could be perceived. However, on the very beggining of irradiation could be noticed slightly higher degradation, caused by the higher charge trapping in the oxide [2]. Shown variations of serial transistor dropout voltage are acceptable and do not deteriorate significantly device's characteristics. Slightly higher sensitivity of unbiased components on ionizing radiation after exposure to higher total doses could be perceived.

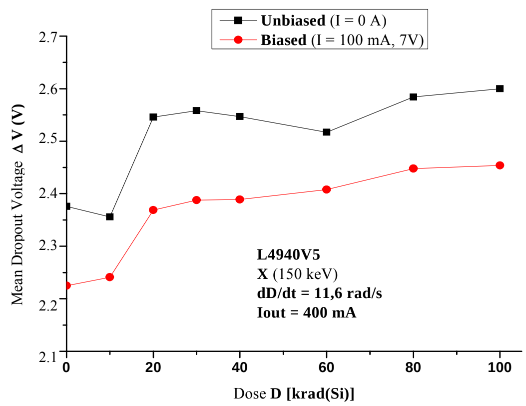

Fig. 6. Change of mean dropout voltage on serial transistor of voltage regulator L4940V5 under influence of X radiation.

Not one of twenty devices, nor in the examination mode without bias, neither during the tests with input voltage and load current, didn't cease functioning, neither output voltage drop bellow the boundary of 4.9 V. The only noticed drawback is slightly higher serial transistor dropout voltage for high bias currents - it reaches 2.15 V for current 700 mA and input voltage 6.5 V, while the manufacturer guarantees maximum dropout voltage 0.9 V, for current 1.5 A and input voltage 7 V [8].

C. *Line regulation characteristics*

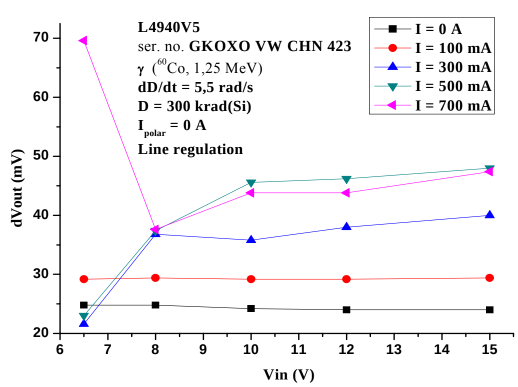

Fig. 7. Line regulation characteristics of unbiased voltage regulator L4940V5 after exposure to γ radiation dose of 300 krad(Si).

In Figs. 7 and 8 are shown line regulation characteristics for integrated circuit L4940V5 after exposure to total ionizing dose 300 krad(Si) without bias and with bias during the irradiation. Reviewing the examination results can be noticed output voltage dropout of 10 - 15 mV after irradiation, dominantly on lower input voltages, from 6.5 V to 8 V, while for the higher values the difference almost cease to exist. Difference in operation unirradiated devices and components that absorbed TID 300 krad(Si) could be noticed for higher voltages and currents, but also in the worst case dropout of output voltage is less then 70 mV. Also after exposure to dose 300 krad(Si), output voltage remains in acceptable boundaries.

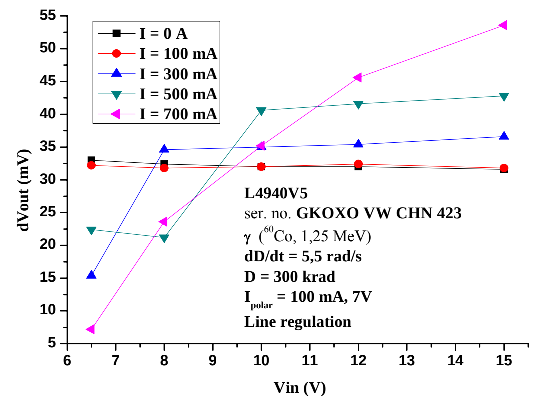

Fig. 8. Line regulation characteristics of biased voltage regulator L4940V5 after exposure to γ radiation dose of 300 krad(Si).

5. Conclusions

Obtained results shows good response of commercial bipolar process "High Density Super Signal/Power Process" (HDS^2/P^2, "Multipower" 20V) for very high ionizing radiation total doses, up to 300 krad(Si), for low and medium energy photons and medium dose rates. Usual value of radiation hardness for commercial voltage regulators is about 30 krad(Si) [12], [13]. The main characteristic of this bipolar process, responsible for high radiation hardness, is vertical construction of bipolar transistors, especially PNP, and procedure of collector junction isolation using N-"wells". The next important characteristic is avoiding of creation of local oxide between collector and emitter, what eliminates the possibility of creation of collector - emitter leakage current. It is necessary to mention that 300 krad(Si) is not ionizing radiation limit for HDS^2/P^2 process, but the limit dictated by the laboratory availability and examination results on complete statistical sample of tested devices.

In γ and X radiation fields "Multipower" HDS^2/P^2 process shown radiation hardness much higher then value requested by the standards of European Space Agency

(ESA), that is 100 krad(Si) [1]. According to the results of presented research, integrated circuits made by HDS^2/P^2 process are completely suitable for applications in ionizing radiation environment.

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*Corresponding author: vvukic@ieent.org